Course Outline

Release 1.0, 21/5/21
Updated 1.1, 15/6/21 — reweighed Lab & Project components; modified due dates for hand-ins

Contents

- Course Details
- Course Summary
- Course Attendance
- Course Timetable
- Course Aims
- Student Learning Outcomes
- Assumed Knowledge
- Teaching Rationale
- Teaching Strategies
- Assessment
- Academic Honesty and Plagiarism
- Course Schedule
- Resources for Students
- Course Evaluation and Development

Course Details

Course Code	COMP4601
Course Title	Design Project B
Units of Credit	6
Course Website	http://cse.unsw.edu.au/~cs4601 (http://cse.unsw.edu.au/~cs4601)
Handbook Entry	http://www.handbook.unsw.edu.au/undergraduate/courses/current/COMP4601.html (http://www.handbook.unsw.edu.au/undergraduate/courses/current/COMP4601.html)

Return to ToC

Course Summary

COMP4601 is a team-based project development course involving the analysis, design and implementation of embedded and/or high performance and/or low power systems using FPGAs. In 2021 the course focus will shift towards the use of high-level synthesis to achieve the course goals.

Teams develop a solution to one of a number of suggested project problems. Project teams are expected to investigate possible approaches, develop their proposal, implement their design, present their solutions, and to report on their investigation and implementation.

The course involves lectures, seminars, lab exercises and project work. Lectures will provide some context for the problems being studied and some background on solution approaches. Students will prepare and assess seminars on advanced topics and related research publications. Project teams will present the results of their investigations and developments.

Return to ToC

Course Attendance

The 21T2 offering of COMP4601 is expected to be online.

- Lectures and seminars will be presented live and will be recorded for viewing at a later time
- Lab sessions during Weeks 1-5 will involve live demonstrations and will be recorded. During Weeks 7-10, you are expected to work on your projects with your team members. Demonstrators will be available online for consultation during lab hours.

During the first 5 weeks, the course covers a fair amount of content at a rapid pace. Keeping up with the readings prior to each week's lectures, attending the lectures to clarify your understanding and attending the labs to actively engage in skills development are essential to picking up the material. During the second half of the course, you are expected to present and to participate in the critical assessment of seminars as well as to contribute to the development of a solution to your project problem. Attendance is expected. Please consider your responsibilities to your colleagues and to yourself in committing to this course.

Return to ToC

Course Timetable

The course timetable is available here .

Return to ToC

Course Aims

Apart from teaching the elements of how to design hardware using high-level synthesis, this course is expected to enhance research skills, sharpen design, implementation and presentation skills, allow students to explore solutions to open-ended problems, and provide opportunities to practice the rapid acquisition of new technical skills with state-of-the-art systems.

Return to ToC

Student Learning Outcomes

By the end of this course, students should be able to:

- rapidly design and implement digital systems that incorporate programable logic,
- explain and put into practice techniques for accelerating computation in hardware,
- independently study advanced techniques in digital design and implementation, and
- document and present their developments in a professional manner.

This course contributes to the development of the following graduate capabilities:

Graduate Capability	Acquired in

scholarship: understanding of their discipline in its interdisciplinary context	Design & implementation tasks; Seminars
scholarship: capable of independent and collaborative enquiry	Design & implementation tasks; Team activities
scholarship: rigorous in their analysis, critique, and reflection	Design & implementation tasks; Presentation & documentation tasks; Lab exercises
scholarship: able to apply their knowledge and skills to solving problems	Design & implementation tasks
scholarship: capable of effective communication	Presentation & documentation tasks; Seminars
leadership: enterprising, innovative and creative	Design & implementation tasks; Team activities
leadership: collaborative team workers	Team activities
professionalism: capable of independent, self-directed practice	Lab exercises; Design & implementation tasks
professionalism: capable of lifelong learning	Seminars
global citizens: culturally aware and capable of respecting diversity and acting in socially just/responsible ways	Team activities

Return to ToC

Assumed Knowledge

The formal pre-requisites for this course are COMP3211 and COMP3601.

It is assumed that, prior to taking this course, students:

- know a hardware description language, such as VHDL or Verilog,
- have experience programming an FPGA,
- have the background to architect solutions to computational problems,
- understand the concepts of sequential programming and know an imperative programming language such as C, and
- understand the purpose and structure of an operating system.

Return to ToC

Teaching Rationale

Hardware design and systems prototyping using field-programmable gate arrays is increasingly important and supports a booming embedded systems and hardware accelerator industry. In order to develop essential skills and to be industrially relevant, computer engineering students need to gain experience designing and prototyping systems and components using programmable logic devices. Increasingly, these devices include hard processors, and therefore require designers to consider the appropriate mix of hardware and software approaches. In recent years much attention has also been given to developing high-level synthesis tools that can enhance the productivity of designers prototyping hardware solutions to computational problems. We therefore endeavour to introduce our students to this important approach to hardware design. The background

necessary to understand the design problem, processors and programmable logic technology will be outlined in classes. Students will work in teams to study and develop solutions using current methodologies to a computationally demanding and relevant problem.

Return to ToC

Teaching Strategies

Formally, the course comprises three lecture hours and three lab hours per week for 10 weeks. However, since this is a 4th year project course, there is an emphasis on working informally with your peers to solve problems. It is expected that you will spend a good deal of time both independently and jointly solving problems you encounter and trying to understand vaguely stated, but important information.

Course participants will study motivating problems during class and undertake practical tasks to gain an appreciation of the main concepts touched upon in the course, namely: high-level synthesis, hardware acceleration, hardware/software co-design, parallel architectures and reconfigurable systems design.The problems to be studied and possible solution approaches will be introduced via lectures. You are expected to prepare for each lecture by reading the relevant chapter before the lecture.

Please read Chapter 1 of the text, Parallel Programming for FPGAs (https://www.cse.unsw.edu.au/~cs4601/21T2/refs/pp4fpgas/kastner-parallel-processing-fpgas.pdf) , before the lecture in Week 1.

In 21T2, a new set of laboratory exercises is provided to facilitate the acquisition of the skills required to make use of the hardware/software provided in the course. Students will work through these exercises and hand in their findings on selected questions each week.

In this course you will partner with fellow students in two types of groups: project and seminar groups. Your project group will decide which problem to study and will jointly work towards an efficient implementation. Your seminar group will study a relevant topic or theme via a set of suggested papers and prepare a joint presentation. The project and seminar tasks both comprise individual and team evaluation components. Overall, your individual efforts will contribute 65% to your final mark in the course.

Project teams are required to report on their progress as they develop solutions to the unique design challenges posed by their projects. A project plan is to be developed and presented to the demonstrators at any time (when teams are ready) but during the scheduled lab sessions in Week 7 at the latest. A final report, demonstration and presentation are due when teams are ready, but during the scheduled lab sessions in Week 10 at the latest. These formal reporting requirements encourage students to manage their project systematically and to plan their work. Feedback on the direction and approach being taken will be provided during the lab sessions in Weeks 7-10.

The preparation and presentation of seminars is intended to provide students with research experience, practice effective communications, and develop professional skills. Audience members are expected to participate in the discussion and to assess the presentation of seminars.

There are no formal examinations in this course.

Return to ToC

Assessment

Assessment in this course will be based on the following:

Criterion	Week due	Contribution
Lab component		**35%**
Week 2 hand in	Friday, Week 2	5% i(ndividual)

Weekly hand ins	Mondays, Weeks 4, 5 & 6	30% i(ndividual)
Seminar component		**30%**
Seminar presentations	Wednesday lectures, Weeks 7-10	10% i(ndividual) + 10% T(eam)
Seminar participation & assessment	Wednesday lectures, Weeks 7-10	10% i
Project component		**35%**
Individual project contribution	Weeks 2-10	10% i(individual)
Project plan (presentation & report)	Lab session, before Week 8	10% T(eam)
Final project presentation, demonstration & report	Lab session, before Week 11	15% T

Individual assessments will be based on individual efforts, individual contributions to team successes, your learning, and ability to adapt to circumstances.

Return to ToC

Academic Honesty and Plagiarism

UNSW has an ongoing commitment to fostering a culture of learning informed by academic integrity. All UNSW staff and students have a responsibility to adhere to this principle of academic integrity. Plagiarism undermines academic integrity and is not tolerated at UNSW. Plagiarism at UNSW is defined as using the words or ideas of others and presenting them as your own.

If you haven't done so yet, please take the time to read the full text of

- UNSW's policy regarding academic honesty and plagiarism (https://student.unsw.edu.au/plagiarism)

The pages below describe the policies and procedures in more detail:

- Student Code Policy (https://www.gs.unsw.edu.au/policy/documents/studentcodepolicy.pdf)
- Plagiarism Policy Statement (https://www.gs.unsw.edu.au/policy/documents/plagiarismpolicy.pdf)
- Plagiarism Procedure (https://www.gs.unsw.edu.au/policy/documents/plagiarismprocedure.pdf)
- Student Misconduct Procedure (https://www.gs.unsw.edu.au/policy/documents/studentmisconductprocedures.pdf)

Return to ToC

Course Schedule

This section explains the weekly schedule of activities, organisational deadlines and due dates for the course.

Weekly schedule

Week	Weekday	Time	Activity
1 - 5	Wednesdays	11:00 - 14:00	Online lecture
	Wednesdays	15:00 - 18:00	Online lab session
	Thursdays	09:00 - 12:00	Repeat lab session
6			No scheduled activities

7 - 10	Wednesdays	11:00 - 14:00	Online seminars
	Wednesdays	15:00 - 18:00	Online project support
	Thursdays	09:00 - 12:00	Online project support

Organisational deadlines

Week	Deadline
2	Preliminary project teams organized
3	Project teams finalised Seminar topics chosen
4	Finalize seminar groups
7	Complete project plans
10	Present project outcomes

Due dates

Week	Weekday	Time	Deliverable
2	Friday	17:00	Week 2 hand-in exercises
4 - 6	Mondays	17:00	Weekly hand-in exercises — Weeks 3, 4 & 5
7	Wednesday	15:00 - 18:00	Project plan presentation & report
	Thursday	09:00 - 12:00	Project plan presentation & report
7 - 10	Wednesdays	11:00 - 14:00	Seminar presentations & assessments
10	Wednesdays	15:00 - 18:00	Final project demos, presentations & reports
	Thursdays	09:00 - 12:00	Final project demos, presentations & reports

Return to ToC

Resources for Students

During the first 5 weeks of lectures, we will be discussing the content of the online book Parallel Programming for FPGAs (https://www.cse.unsw.edu.au/~cs4601/21T2/refs/pp4fpgas/kastner-parallel-processing-fpgas.pdf) by Ryan Kastner, Janarbek Matai and Stephen Neuendorfer . Lab exercises will be also be based on exercises suggested in this text. We will use the 2020.1 version of Vivado and Vitis tools from Xilinx and target the Xilinx Zynq 7020 device hosted on ZedBoards. Students will be guided in their uptake of the tools via Xilinx tutorials and guides prepared by the teaching staff.

Students will need to refer to research papers, product data sheets, application notes, standards, system documentation, reference books and technical articles to gain the background needed to design and implement the project systems. Some of these references will be identified during the course. Please ask the lecturer and/or demonstrator for assistance if you are lost.

Return to ToC

Course Evaluation and Development

Student feedback on this course will be obtained via electronic survey (myExperience) at the end of session and will be used to make improvements to the course. **Students are encouraged to provide informal feedback during the session and to let the lecturer in charge know of any problems as soon as they arise** . Every reasonable effort to address concerns will be made.

In 2021, the course is being updated to focus on high-level synthesis in FPGA design. This is driven by market changes - a perception that HLS has reached a maturity that allows it to be used with confidence, while benefiting from more rapid exploration of alternative hardware designs - as well as a desire to cover relevant design techniques in our undergraduate offering. Since HLS is new to students, the first part of the course necessarily requires more focus on lectures and laboratory practice. Despite this shift, it is hoped that we can also manage to carry out meaningful project work and expose students to seminar preparation and presentation. Your efforts to trial the new approach, which may not yet be perfect, and to provide constructive feedback are appreciated. The 2020 myExperience feedback included comments that communication wasn't great and that feedback was not timely. I plan to make weekly announcements of upcoming due dates and any updates/changes to the course. We will also have additional demonstrators on hand this term to help in the labs, with marking weekly hand-ins, and with advising during the project development period. Please let me know if we could improve!

Return to ToC

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