Course Outline (last updated 17 Feb) Student

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Course Details

Course Code	COMP4601
Course Title	Design Project B
Units of Credit	6
Course Website	http://cse.unsw.edu.au/~cs4601 (http://cse.unsw.edu.au/~cs4601)
Handbook Entry	http://www.handbook.unsw.edu.au/undergraduate/courses/current/COMP4601.html (http://www.handbook.unsw.edu.au/undergraduate/courses/current/COMP4601.html)

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Course Summary

COMP4601 is a team-based project development course involving the design and implementation of embedded and/or high performance and/or low power systems using FPGAs.

Teams develop a solution to one of a number of suggested project problems. Project teams are expected to investigate possible approaches, develop their proposal, implement their design, present their solution, and to report on their investigation and implementation.

The course involves lectures, seminars, lab exercises and project work. Lectures will provide some context for the problems being studied and some background on solution approaches. Students will prepare and assess seminars on related research publications. Project teams will present the results of their investigations and developments.

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Course Attendance

Since COMP4601 is a team-based project design course, students are expected to attend all classes to help form and contribute to the progress of their team. Your ability to assist the team will partially depend upon your understanding of the hardware and software introduced through guided lab exercises and the techniques discussed in lectures. Furthermore, students are expected to contribute to the presentation of a group seminar. For these reasons, if you are unable to attend classes after Week 2, it is recommended that you withdraw from the course as soon as possible.

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Course Timetable

The course timetable is available here (/COMP4601/20T1/timetable) .

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Course Aims

This course is expected to enhance research skills, sharpen design, implementation and presentation skills, allow students to explore solutions to open-ended problems, and provide opportunities to practice the rapid acquisition of new technical skills with state-of-the-art systems.

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Student Learning Outcomes

By the end of this course, students should be able to:

- design and implement digital systems that incorporate programable logic,
- explain and put into practice techniques for accelerating computation in hardware,
- independently study advanced techniques in digital design and implementation, and
- document and present their developments in a professional manner.

This course contributes to the development of the following graduate capabilities:

Graduate Capability	**Acquired in**
scholarship: understanding of their discipline in its interdisciplinary context	Design & implementation tasks; Seminars
scholarship: capable of independent and collaborative enquiry	Design & implementation tasks; Team activities
scholarship: rigorous in their analysis, critique, and reflection	Design & implementation tasks; Presentation & documentation tasks; Lab exercises

scholarship: able to apply their knowledge and skills to solving problems	Design & implementation tasks
scholarship: capable of effective communication	Presentation & documentation tasks; Seminars
leadership: enterprising, innovative and creative	Design & implementation tasks; Team activities
leadership: collaborative team workers	Team activities
professionalism: capable of independent, self-directed practice	Lab exercises; Design & implementation tasks
professionalism: capable of lifelong learning	Seminars
global citizens: culturally aware and capable of respecting diversity and acting in socially just/responsible ways	Team activities

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Assumed Knowledge

The formal pre-requisites for this course are COMP3211 and COMP3601.

It is assumed that, prior to taking this course, students:

- know a hardware description language,
- have experience programming an FPGA,
- have the background to architect solutions to computational problems,
- understand the concepts of sequential programming and know an imperative programming language such as C, and
- understand the purpose and structure of an operating system.

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Teaching Rationale

Hardware design and systems prototyping using field-programmable gate arrays is increasingly important and supports a booming embedded systems and hardware accelerator industry. In order to develop essential skills and to be industrially relevant, computer engineering students need to gain experience designing and prototyping systems and components using programmable logic devices. Increasingly, these devices include hard processors, and therefore require designers to consider the appropriate mix of hardware and software approaches. The background necessary to understand the design problem, processors and programmable logic technology will be outlined in classes. Students will work in teams to study and develop solutions using current methodologies to a computationally demanding and relevant problem.

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Teaching Strategies

Formally, the course comprises three lecture hours and three lab hours per week for 10 weeks. However, since this is a 4th year project course, there is an emphasis on working informally with your peers to solve problems. It is expected that you will spend a good deal of time both independently and jointly solving problems you encounter and trying to understand vaguely stated, but important information.

Course participants will study motivating problems during class and undertake practical tasks to gain an appreciation of the main concepts touched upon in the course, namely: hardware acceleration, hardware/software co-design, parallel architectures and reconfigurable systems design.The problems to be studied and possible solution approaches will be introduced via lectures.

A suite of laboratory exercises is provided to facilitate the acquisition of the skills required to make use of the hardware/software provided in the course. Students will keep a log of their experiences, observations, questions and discoveries as they are guided through the exercises.

In this course you will partner with fellow students in two types of groups: project and seminar groups. Your project group will decide which problem to study and will jointly work towards an efficient implementation. Your seminar group will study a relevant topic or theme and prepare a joint presentation. The project and seminar tasks both comprise individual and team evaluation components. Overall, your individual efforts will contribute 65% to your final mark in the course.

Project teams are required to report on their progress as they develop solutions to the unique design challenges posed by their projects. A project plan is to be developed and presented to the class during Week 5 - a written plan will also be submitted at this stage. A design review involving a demonstration of progress will take place in Week 7 this year. A final report, demonstration and presentation are due in Week 11. These formal reporting requirements encourage students to manage their project systematically and to plan their work. Regular feedback on the direction and approach being taken will be provided during the lab sessions.

The preparation and presentation of seminars is intended to provide students with research experience, practice effective communications, and develop professional skills. Audience members are expected to participate in the discussion and to assess the presentation of seminars.

There are no formal examinations in this course.

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Assessment

Assessment in this course will be based on the following:

Criterion	Week due	Contribution
Lab component		**15%**
Lab logbook	Friday, Week 4	15% i(ndividual)
Seminar component		**35%**
Seminar presentations	Mondays, Weeks 7-10	15% i(ndividual) + 5% T(eam)
Seminar participation & assessment	Mondays, Weeks 7-10	15% i
Project component		**50%**
Individual project contribution	Weeks 2-10	20% i(individual)
Project plan (presentation & report)	Friday, Week 5	5% T(eam)
Design review (discussion & report)	Friday, Week 7	5% T
Final project presentation, demonstration & report	Monday, Tuesday & Wednesday, Week 11	20% T

Individual assessments will be based on individual efforts, individual contributions to team successes, your learning, and ability to adapt to circumstances.

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Academic Honesty and Plagiarism

UNSW has an ongoing commitment to fostering a culture of learning informed by academic integrity. All UNSW staff and students have a responsibility to adhere to this principle of academic integrity. Plagiarism undermines academic integrity and is not tolerated at UNSW. Plagiarism at UNSW is defined as using the words or ideas of others and presenting them as your own.

If you haven't done so yet, please take the time to read the full text of

- UNSW's policy regarding academic honesty and plagiarism (https://student.unsw.edu.au/plagiarism)

The pages below describe the policies and procedures in more detail:

- Student Code Policy (https://www.gs.unsw.edu.au/policy/documents/studentcodepolicy.pdf)
- Plagiarism Policy Statement (https://www.gs.unsw.edu.au/policy/documents/plagiarismpolicy.pdf)
- Plagiarism Procedure (https://www.gs.unsw.edu.au/policy/documents/plagiarismprocedure.pdf)
- Student Misconduct Procedure (https://www.gs.unsw.edu.au/policy/documents/studentmisconductprocedures.pdf)

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Course Schedule

Week	Day	Activity
1	Monday (17/2)	Introductory lecture
		Preliminary project teams decided
	Friday	Lab 1
2	Monday (24/2)	Image processing lecture
	Friday	Labs 2 & 6
		Finalize project teams
3	Monday (2/3)	Communications lecture
		Deep learning lecture
		Finalize seminar groups
	Friday	Custom IP lab
4	Monday (9/3)	Project time in lab
	Friday	**Lab logbooks collected (https://www.cse.unsw.edu.au/~cs4601/20T1/labs/comp4601-lab-familiarization-20T1.pdf)**
		Project time in lab

5	Monday (16/3)	Project time in lab
	Friday	**Project plan presentations in lab (https://www.cse.unsw.edu.au/~cs4601/20T1/protected/proj-reports.html#W5)**
		Project plans due in wiki (https://www.cse.unsw.edu.au/~cs4601/20T1/protected/proj-reports.html#W5)
6	Monday (23/3)	Consolidation/Project time in lab
	Friday	Consolidation/Project time in lab
7	Monday (30/3)	Seminars x2 in OMB-150
	Friday	**Progress check in lab (https://www.cse.unsw.edu.au/~cs4601/20T1/protected/proj-reports.html#W7)**
8	Monday (6/4)	Seminars x2 in OMB-150
	Friday	Good Friday holiday
9	Monday (13/4)	Easter Monday holiday
	Friday	Project time in lab
10	Monday (20/4)	Seminars x3 in OMB-150
	Friday	Project time in lab
11	Monday (27/4)	**Project presentations in OMB-150 (https://www.cse.unsw.edu.au/~cs4601/20T1/protected/proj-reports.html#W11)**
	Tuesday	**Project demos in lab (https://www.cse.unsw.edu.au/~cs4601/20T1/protected/proj-reports.html#W11)**
	Wednesday	**Project reports due in wiki (https://www.cse.unsw.edu.au/~cs4601/20T1/protected/proj-reports.html#W11)**

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Resources for Students

There is no prescribed text for this course. However, students will need to refer to research papers, product data sheets, application notes, standards, system documentation, reference books and technical articles to gain the background needed to design and implement the project systems. Some of these references will be identified during the course. Please ask the lecturer and/or demonstrator for assistance if you are lost.

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Course Evaluation and Development

Student feedback on this course will be obtained via electronic survey (myExperience) at the end of session and will be used to make improvements to the course. Students are encouraged to provide informal feedback during the session and to let the lecturer in charge know of any problems as soon as they arise. Every reasonable effort to address concerns will be made.

Students have commented that they enjoyed the in-depth exposure to reconfigurable technology and project experience gained in Design Project B. With the change in course duration, in 2019 we began to examine the industry shift towards productivity tools, such as the use of high-level synthesis to create programmable logic accelerators. To ease the learning burden and provide more guidance, we also provided demonstrations of the tools via lab walk-throughs in Weeks 1 & 2. Seminars were presented by panels so as to reduce the individual load and provide a more coherent view of each seminar theme. These changes to the course helped lessen the impact of shortening the course duration.

In 2020, we have made some further changes to cater for students who are late arriving, we have attempted to clarify the schedule (see above) and slightly reduced the assessment load as far as labs are concerned. Furthermore, 2020 will be the first offering to benefit from the course wiki, which was started in 2019. While not intended to set an example of the quality expected in the course, this resource should provide some additional guidance for project teams. Similarly, the seminar presentations from 2019 will be made available to provide a guide for the 2020 cohort.

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