Course Outline

COMP4601
Design Project B
Semester 1 2015

Contents

- Course Staff
- Course Details
- Course Summary
- Course Aims
- Student Learning Outcomes
- Assumed Knowledge
- Teaching Rationale
- Teaching Strategies
- Assessment
- Academic Honesty and Plagiarism
- Course Schedule
- Resources for Students
- Course Evaluation and Development

Course Staff

Contact Details

Staff Name	Role	Email	Phone
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Consultations

Please email me to arrange a suitable meeting time.

Course Details

Course Code:	COMP4601
Course Title:	Design Project B
Units of Credit:	6
Course WebSite:	http://www.cse.unsw.edu.au/~cs4601/
Handbook Entry:	http://www.handbook.unsw.edu.au/undergraduate/courses/2015/COMP4601.html

Course Summary

COMP4601 is a team-based project development course involving the design and implementation of embedded and high performance or low power systems using FPGAs.

In 2015, teams will develop a solution to one of a number of suggested project problems. Project teams are expected to investigate possible approaches, develop their proposal, implement their design, present their solution, and to report on their investigation and implementation.

The course will involve lectures, seminars and lab sessions. Lectures will provide the context for the problems being studied. Students will prepare seminars on recent research publications. Project teams will present the results of their investigations and developments.

Course Aims

This course is expected to enhance research skills, sharpen design, implementation and presentation skills, allow students to explore solutions to open-ended problems, and provide opportunities to practice the rapid acquisition of new technical skills with state-of-the-art systems.

Student Learning Outcomes

By the end of this course, students should be able to:

- design and implement digital systems using configurable logic,
- be able to distinguish when processor-based and logic-based solutions to computing problems are called for,
- explain and put into practice techniques for accelerating computation in hardware,
- independently study advanced techniques in digital design and implementation, and
- document and present their developments in a professional manner.

This course contributes to the development of the following graduate attributes:

Graduate Attribute	Where Acquired
an in-depth engagement with relevant disciplinary knowledge in its interdisciplinary context	Design & implementation tasks; Seminar
the capacity for enterprise, initiative and creativity	Design & implementation tasks
the skills required for collaborative and multidisciplinary work	Team activities
the skills of effective communication	Presentation & documentation tasks

Assumed Knowledge

The formal pre-requisites for this course are COMP3211 and COMP3601.

It is assumed that, prior to taking this course, students:

- know a hardware description language,
- have experience programming an FPGA,
- have the background to architect solutions to computational problems
- understand the concepts of sequential programming and know an imperative programming language such as C, and
- understand the purpose and structure of an operating system.

Teaching Rationale

Hardware design and systems prototyping using field-programmable gate arrays is increasingly important and supports a booming embedded systems industry. In order to develop essential skills and to be industrially relevant, Computer Engineering students need to gain experience designing and implementing systems and components using programmable logic devices. Increasingly, these devices include hard processors, and therefore require designers to consider the appropriate mix of hardware and software approaches. The background necessary to understand the design problem and programmable logic technology will be outlined in classes. Students will work in teams to study and develop solutions using current methodologies to a computationally demanding and relevant problem.

Teaching Strategies

Formally, the course comprises three lecture hours and two lab hours per week for 12 weeks. However, since this is a 4th year project course, there will be an emphasis on working informally with your team member(s) to design solutions to the chosen problem. It will also be expected that you may need to spend a good deal of time independently and/or jointly solving problems you encounter and trying to understand vaguely stated vital information.

The course and particular problems to be studied will be introduced in Weeks 1-3 via lectures. Early in this period, your team will choose the project you will work on. You will also be assigned a seminar paper to present and commence work on laboratory exercises to familiarise you with the hardware/software used in the course.

You will have the opportunity to select your team partner (to form teams of 2) and to select the project you will work on. It is hoped that these degrees of freedom will encourage strong and satisfying collaboration and enhance co-operation in acquiring necessary skills as well as in developing solutions.

Project teams are required to report on their progress as they develop solutions to the design challenges posed by their projects. Reports are to be submitted on the Project Plan (in Week 3), a Design Review (Week 6), the Implementation & Test Plan (Week 9), and a Final Report (Week 12). These formal reporting requirements encourage students to manage their project systematically and to actually plan their work. Regular feedback on the direction and approach being taken will be provided during the lab session in even numbered weeks. Project presentations and demonstrations will occur during Week 13.

A schedule of 5 laboratory exercises has been developed to facilitate the acquisition of the skills required to make use of the hardware/software provided in the course. At the completion of each lab, students are required to reflect upon their learning via a brief written report.

The preparation and presentation of seminars is intended to provide students with research experience, practice effective communications, and develop professional skills. Audience members are expected to participate in the discussion and to assess the presentation of the seminar.

At the completion of the course the lecturer will interview students individually to gain an understanding of the

unique experiences they have had during the course. This helps formulate new approaches and guides the individual assessment of students scored as a team.

Note: Given the complexity of teaching a group of students with diverse backgrounds and different projects, the lecturer may revise or take detours from the plans stated in this Course Outline in order to better achieve the course objectives.

Assessment

Assessment in this course will be based on the following:

Week(s)	Criterion	Contribution
2-13	Individual project contribution	20% i(individual)
3	Project plan	4% T(eam)
4-12	Seminar	15% i
4-12	Seminar participation & assessment	10% i
5	Report on AES Labs 1, 2, 3 & 6	7.5% i
6	Design review	8% T
7	Report on Custom IP lab	7.5% i
9	Implementation & test plan	8% T
12	Final report	12% T
13	Project presentation & demo	8% T

Individual assessments will be based on individual efforts made to contribute to team successes, your learning, and ability to adapt to circumstances. All students will be interviewed on Friday 5 June.

Academic Honesty and Plagiarism

Plagiarism is defined as "using the words or ideas of others and presenting them as your own". UNSW and CSE treat plagiarism as academic misconduct, which means that it carries penalties as severe as being excluded from further study at UNSW. There are several on-line sources to help you understand what plagiarism is and how it is dealt with at UNSW:

- Learning Centre: Plagiarism and Academic Integrity
- MyUNSW: Plagiarism and Academic Misconduct
- CSE: Addendum to UNSW Plagiarism Guidelines
- CSE: Yellow Form (whose terms you have agreed to)

Make sure that you read and understand these. Ignorance is not accepted as an excuse for plagiarism.

Course Schedule

Lectures are scheduled to occur in Weeks 1-3 and as needed thereafter.

Teams will prepare and submit their Project Plan by Week 3. Individual discussions will be held with teams during the lab sessions in even-numbered weeks.

Students will commence lab work by Week 2 and submit reports on their impressions & implementations during Weeks 5 and 7.

During the lecture periods of Weeks 4-12, individual students will conduct seminars on recent research publications assigned during Weeks 1-2. Audience members are expected to participate in the discussion and to assess the presentation of the seminar.

Further project reports are to be submitted during Weeks 6, 9 and 12. Feedback will be provided in the following meetings.

During the lecture and lab sessions of Week 13, teams will present and demonstrate their solutions to the problems they studied.

Students are required to attend an exit interview lasting approximately 20 mins on Friday 5 June (Week 13).

Resources for Students

There is no prescribed text for this course. However, students will need to refer to product data sheets, application notes, standards, system documentation, reference books and technical articles to gain the background needed to design and implement the project systems. Some of these references will be identified during the course. Please ask the lecturer for assistance if lost.

Course Evaluation and Development

Student feedback on this course will be obtained via electronic survey (CATEI) at the end of session and will be used to make improvements to the course. Students are encouraged to provide informal feedback during the session and to let the lecturer in charge know of any problems as soon as they arise. Every reasonable effort to address concerns will be made.

Following significant revision to the course in 2014 to accommodate new FPGA boards and software, and to engage students more actively in learning and presenting material via seminars, we have this year decided to increase the amount of feedback students and teachers are expected to provide in the lab and project components of the course. It is hoped that this will better keep students on track and help them obtain more useful experiences from their learning activities.