49 DESIGN AUTOMATION CONFERENCE

SAN FRANCISCO, CA, USA

CHA'N'GE

Guaranteed Fault Recovery Time for FPGA-based TMR Circuits Employing Partial Reconfiguration

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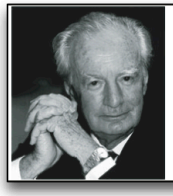

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POLITECNICO DI MILANO

Outline

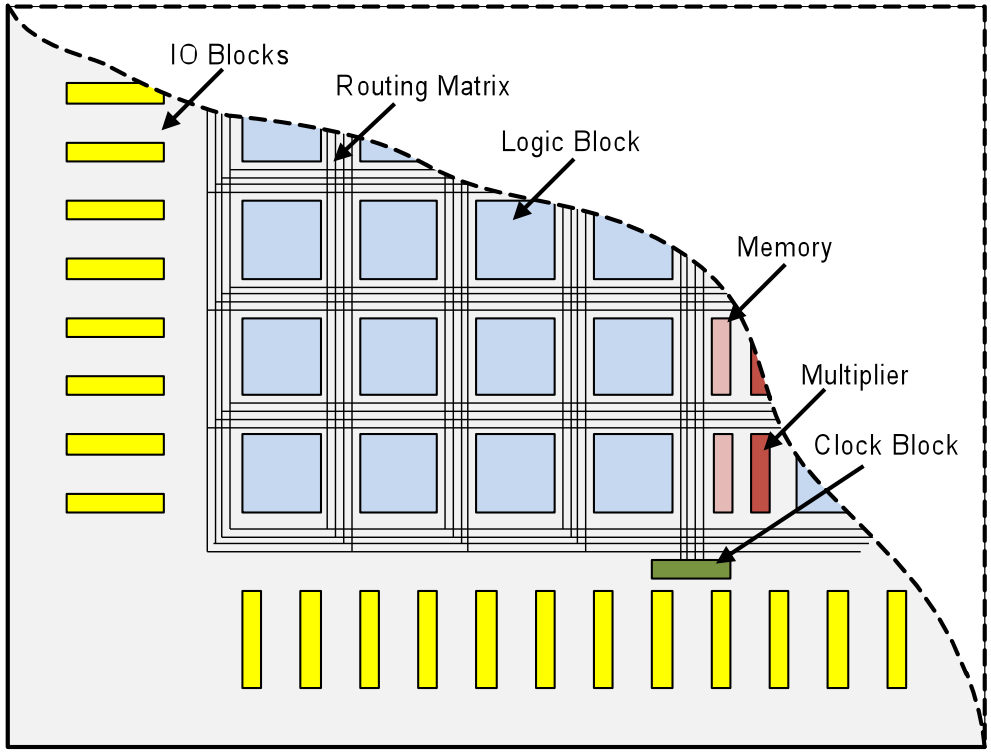
- Motivation & Background
- Objectives & Approach
- Our technique
- Results so far
- Work in progress

Motivations

- Space-based systems are increasingly important in our daily lives
  - Systems with bandwidths of 10-60 Gb/s and throughput of up to 1 TOPs are being planned
  - Next gen systems are required to be re-programmable during operation
- Off-the-shelf SRAM-based FPGAs are ideally suited to meeting these demands

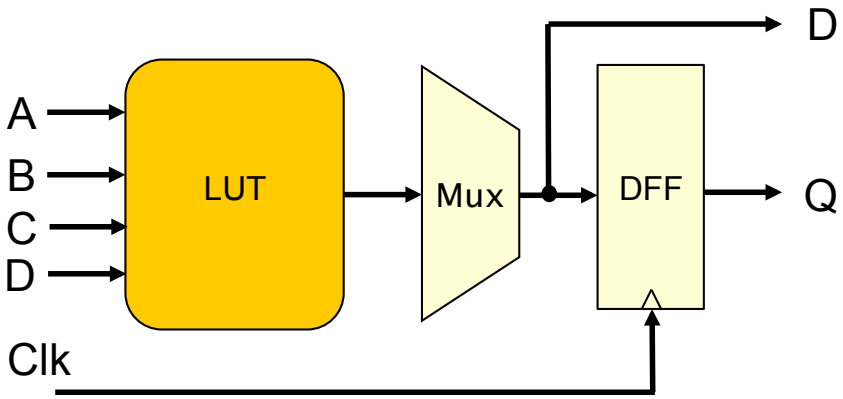
FPGA Architecture

- Device cut-away



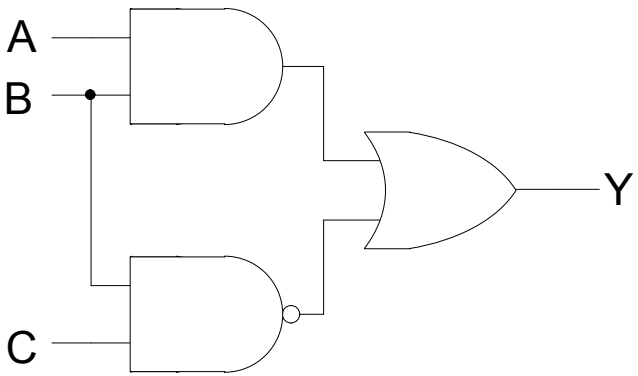
FPGA Architecture

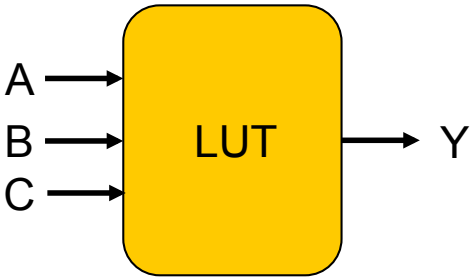
- Logic Block structure



FPGA Architecture

- Logic function implementation

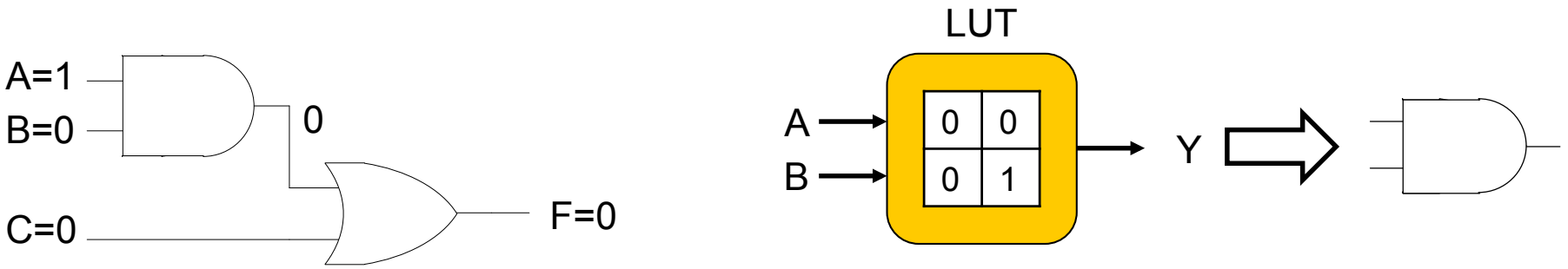




A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

FPGA Susceptability to SEUs

- BUT…FPGAs are particularly susceptible to radiation-induced Single Event Upsets (SEUs)
  - Deposited charge causes a change of state in dynamic circuit elements
  - Affects both datapath and configuration memory



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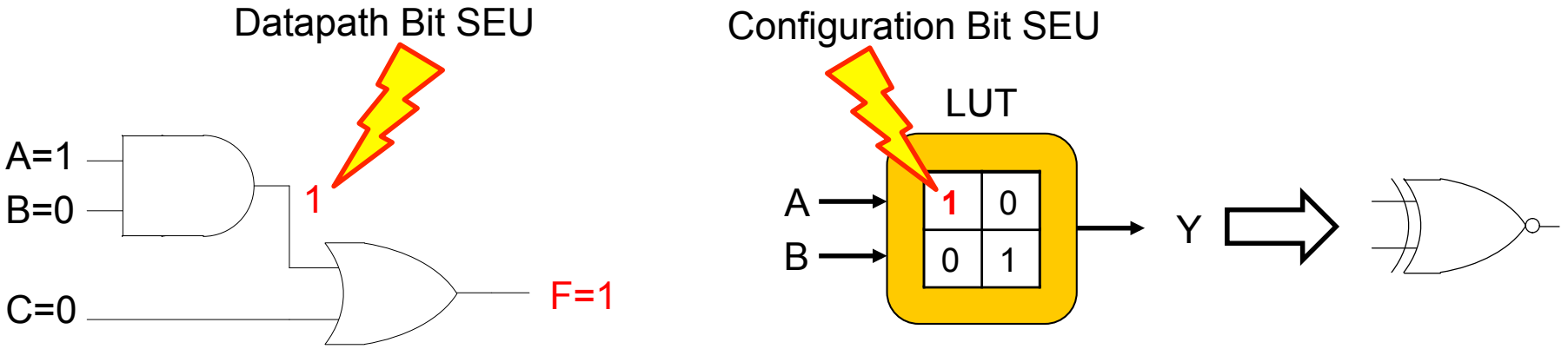


FPGA Susceptability to SEUs

- SEU occurrence increases with orbit radius

Orbit	SEUs/day	MTTU (s)
LEO (560 km)	4.09	2.11×10^4
Polar (833 km)	1.49×10^4	5.81
GPS (20,200 km)	5.46×10^4	1.58
Geosynchronous (36,000 km)	6.2×10^4	1.39

Predictions for Virtex-4 (XC4VLX200) [Engel et al., 2006]

FPGA Susceptability to SEUs

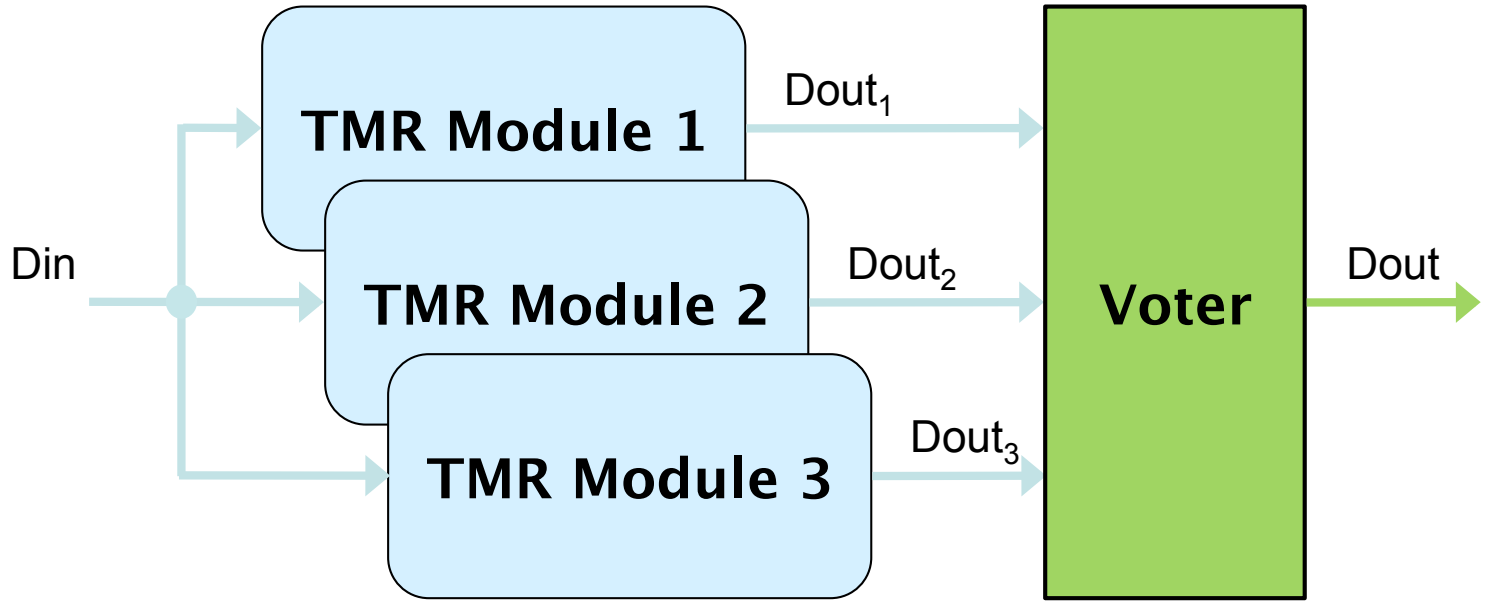
- SEUs have more significant impact as transistor sizes shrink

Device Family	Technology Node	Total Events	1-Bit Events	2-Bit Events	3-Bit Events	4-Bit Events
Virtex	250 nm	241,166	241,070 (99.996%)	96 (0.004%)	0 (0%)	0 (0%)
Virtex-II	150 nm	541,823	523,280 (98.42%)	6,293 (1.16%)	56 (0.01%)	3 (0.001%)
Virtex-II Pro	130 nm	10,430	10,292 (98.68%)	136 (1.30%)	2 (0.02%)	0 (0%)
Virtex-4	90 nm	152,577	147,902 (96.44%)	4,567 (2.99%)	78 (0.05%)	8 (0.005%)

Event distribution due to proton radiation @63.3 MeV [Quinn et al., 2005]

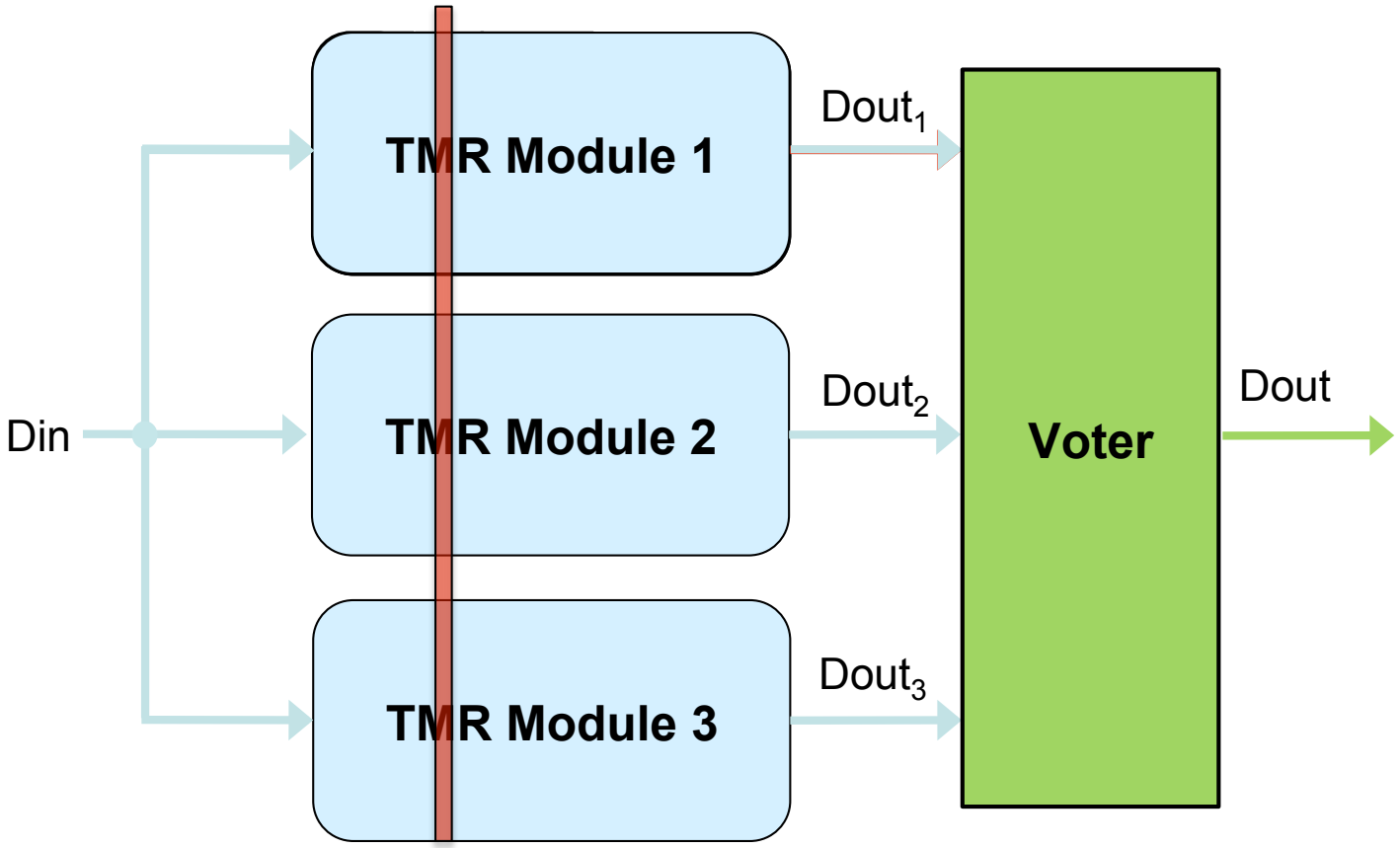
SEU mitigation in FPGAs

- Triple Modular Redundancy (TMR)



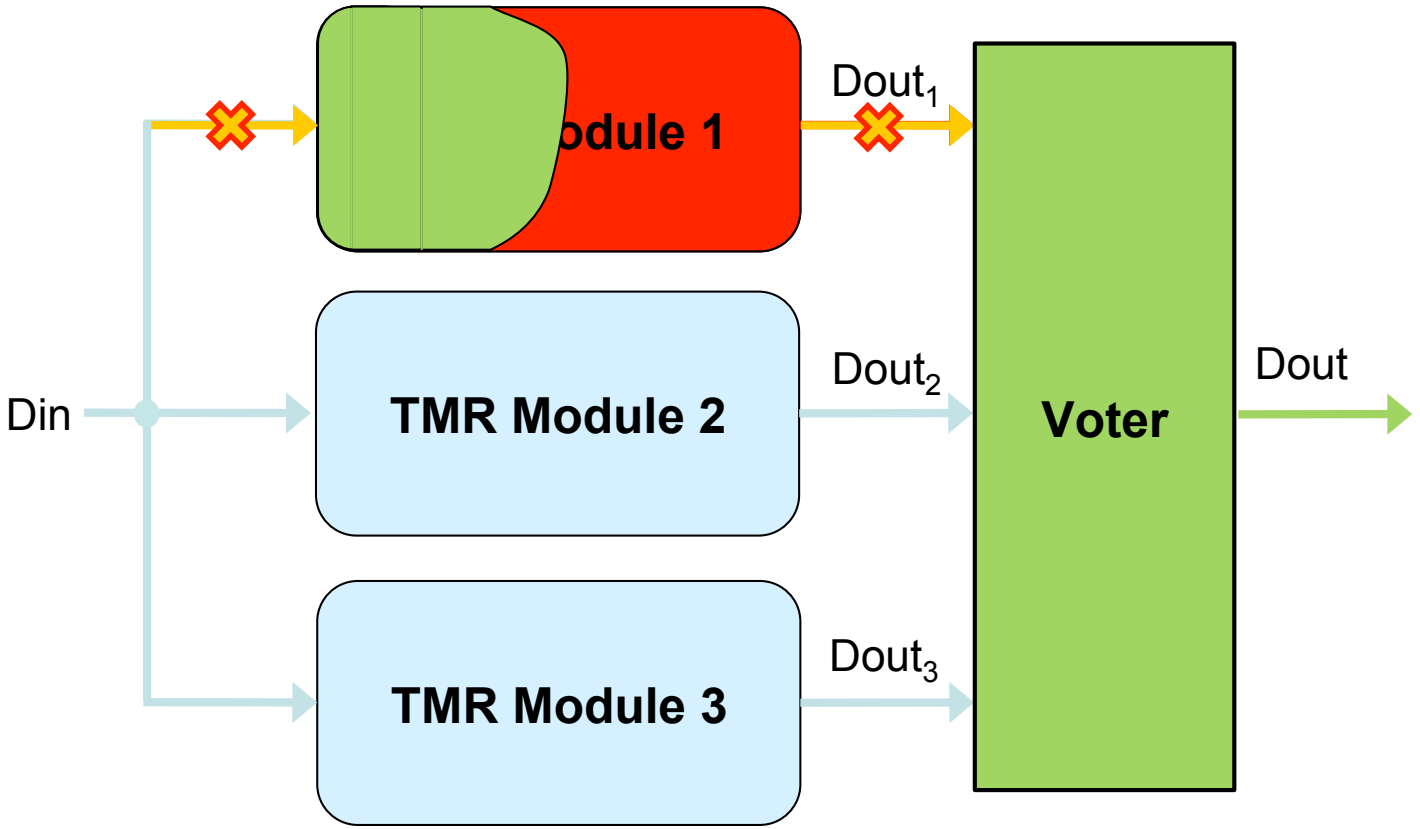
SEU mitigation in FPGAs

- Triple Modular Redundancy (TMR)
  - Eliminate configuration errors by scrubbing



SEU mitigation in FPGAs

- Triple Modular Redundancy (TMR)
  - Eliminate configuration errors by scrubbing
  - Or by dynamic modular reconfiguration



Resynchronisation approaches

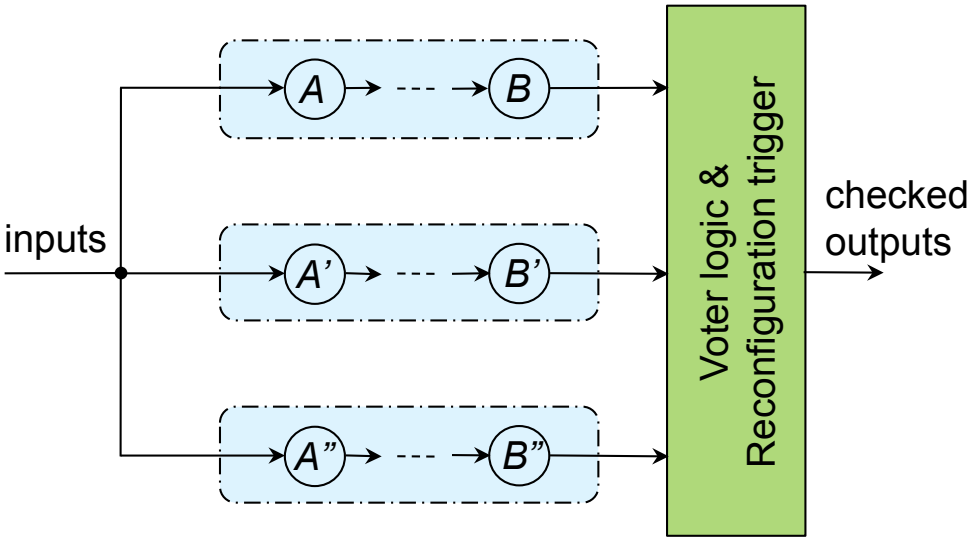
- System reset may take too long and cause data to be lost
- Copying state between modules is infeasible – too many wires & too much control
- Checkpointing state is complicated and costly – too much memory & control
- Predicting future state is complicated and limited – only feasible for small FSMs

Objectives

- Develop a general approach
- Protect FPGA circuits from SEUs
- Bound the maximum time to detect and recover from configuration memory errors

Acyclic circuits

- Simplest case:
  - Pipeline or linear filter
  - Streamed data



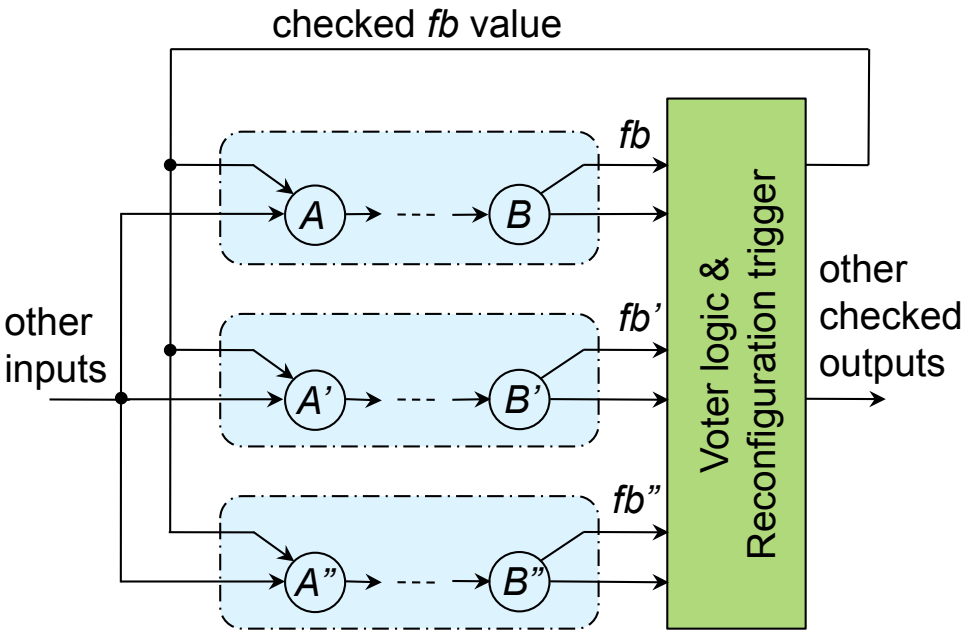
- Represent as acyclic DFG
  - Node = Op [+ Reg]
  - Edge = Data transfer
- >2 successive errors trigger reconfiguration of faulty module
- Time to detect fault:

$$t_{D\_MAX} \leq N \text{ clock cycles}$$

- Time to recover from fault:

$$\leq 2\,t_{D\_MAX} + t_R \text{ clk cycles}$$

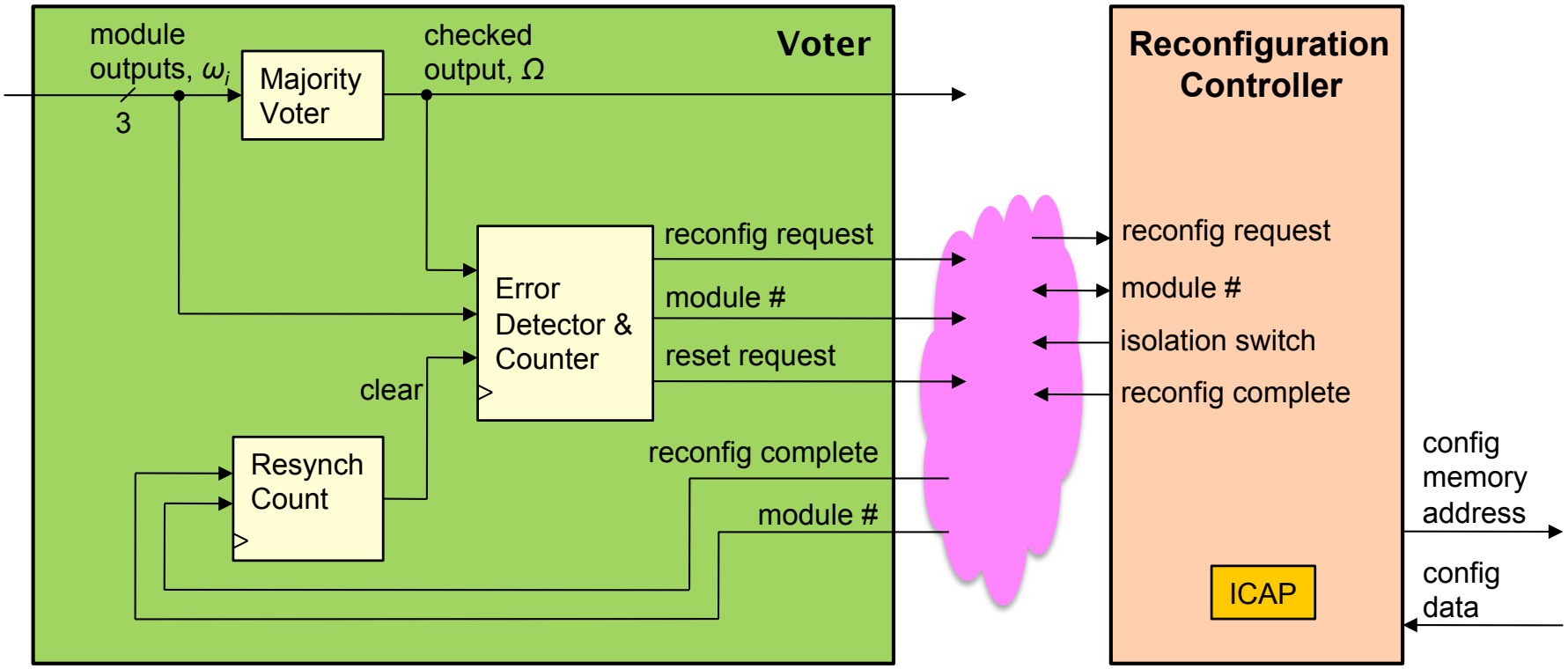
Cyclic circuits



- The cause of persistent faults in cyclic components cannot be determined
- The correct state cannot be set by presenting new inputs to the circuit

⇒ Cut feedback edges & vote on them; recycle *fb* as an input to an otherwise acyclic component

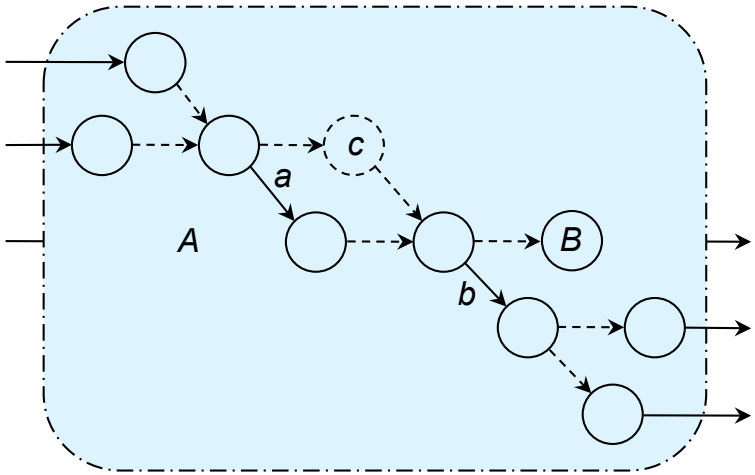
Reconfiguration control



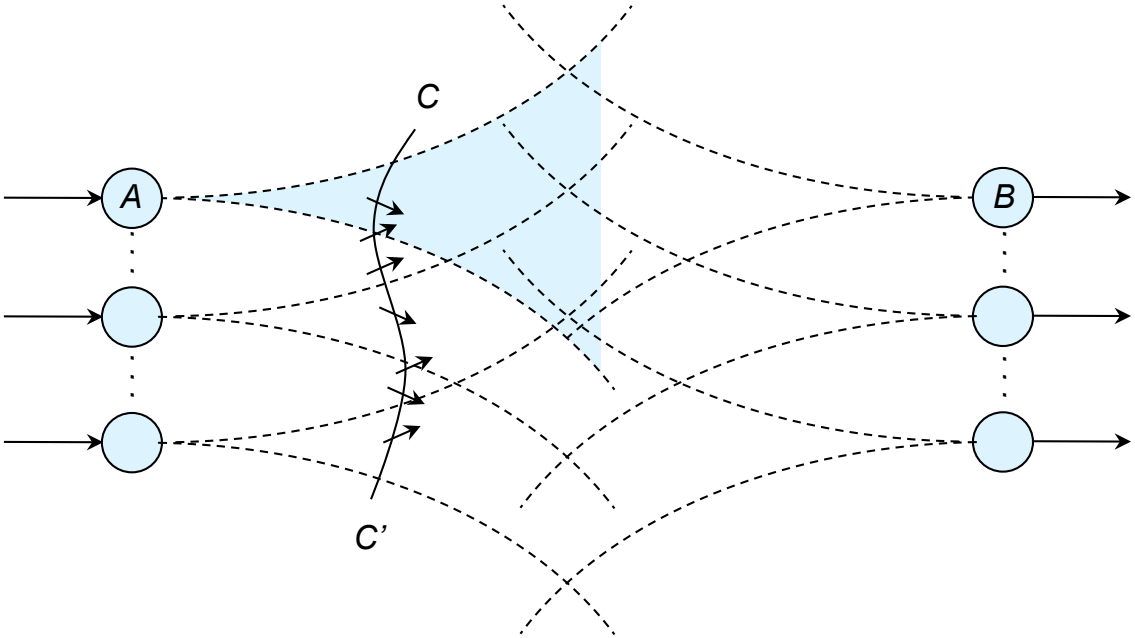
TM outputs, $\omega_i = \{A, B, C\}$, ω_i a vector of all output bits from module *i*
$\Omega = A \cdot B + B \cdot C + A \cdot C$
$error_i = \omega_i \oplus \Omega$
reset request = $\omega_j \oplus \omega_k$ while ω_i reconfiguring

Partitioning a circuit

- Fault detection and recovery times are affected by component latency
- Recovery time is also affected by reconfiguration time, which depends upon component size
- Internal structure of acyclic components does not affect correctness
  - Require voter to check all outputs
  - Ensure all inputs arrive at each module in the same cycle



Partitioning a circuit



- Partitioning is feasible when the area & latency of DFG nodes are known
  - Probably requires synthesized & tech-mapped netlists
- Explore the DFG breadth-first:
  - Advance wavefront *CC'* of included nodes
  - Iteratively update the area & latency included in the partition
  - Halt advance before maximum delay $2t_{D\_MAX} + t_R$ exceeded
  - Continue with the outputs of the previous partition

Preliminary results

- Simulation using a simple encryption engine as the TM component
- Easier to implement and faster to resyn-chronise than [Azambuja et al., 2009]
  - No need to include state prediction table
  - No need to wait for predicted state to be entered before resynching

Directions for further work

- Developing automated partitioning and layout tools based on VPR
- Benchmarking the technique on common signal processing circuits
- Implementing FPGA-based systems with large numbers of reconfigurable regions
- Autonomous approaches to detecting and mitigating faults