Microkernels and L4

Introduction

COMP9242 2006/S2 Week 1

Why Microkernels?

Monolithic kernel

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- Kernel has access to everything
  - ➜ all optimisations possible
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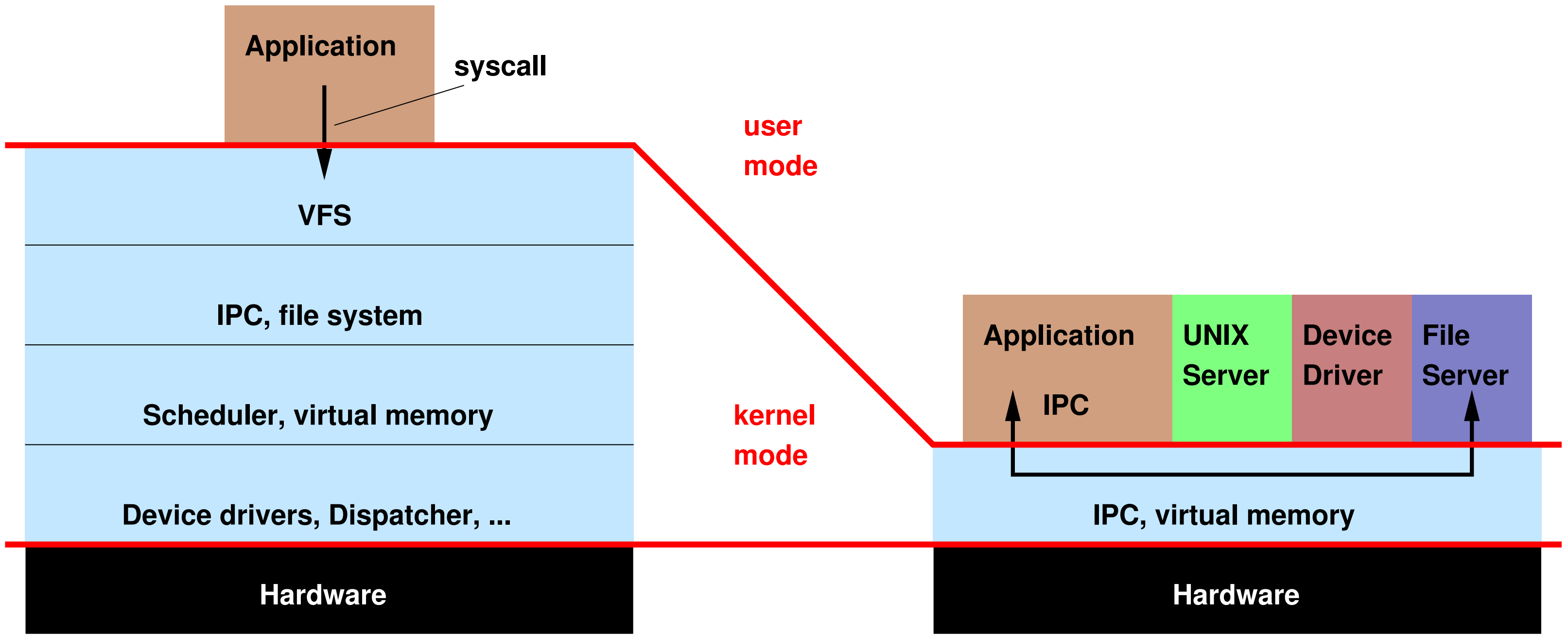
- Can be extended by simply adding code
- Cost: Complexity
  - ➜ growing size
  - ➜ limited maintainability

MICROKERNEL: IDEA

- Small kernel providing core functionality
  ➜ only code running in privileged mode
- Most OS services provided by user-level servers
- Applications communicate with servers via message-passing IPC



TRUSTED COMPUTING BASE

The part of the system which must be trusted to operate correctly

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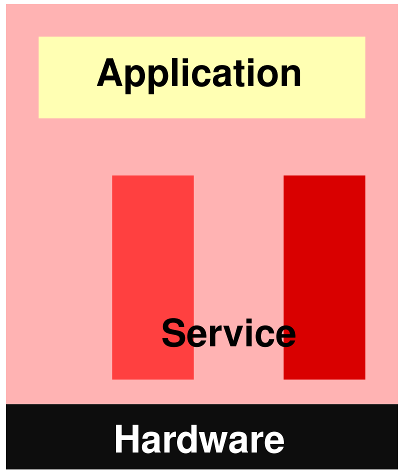

System: traditional
embedded

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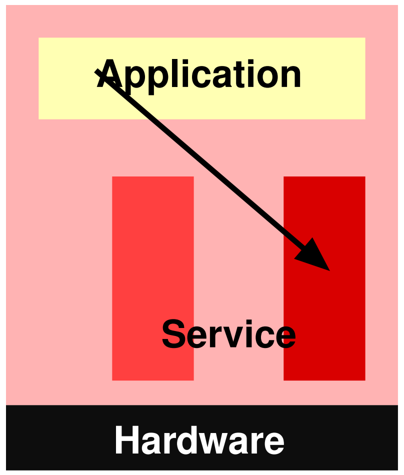

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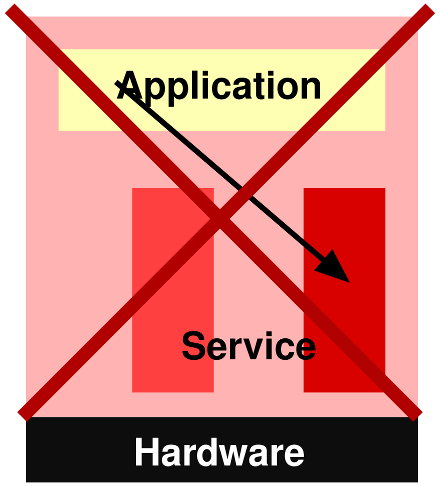

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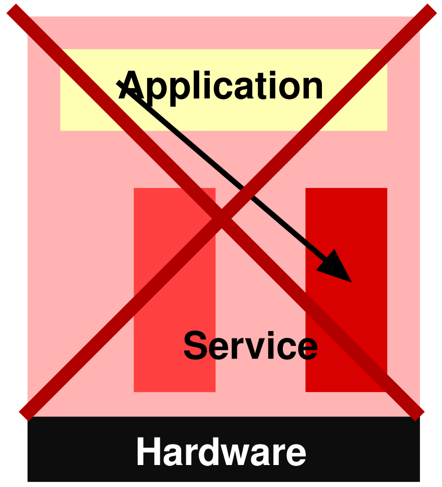

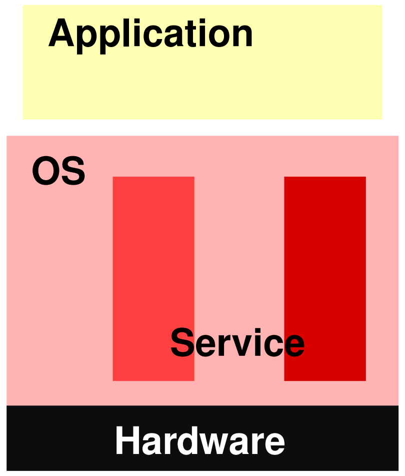

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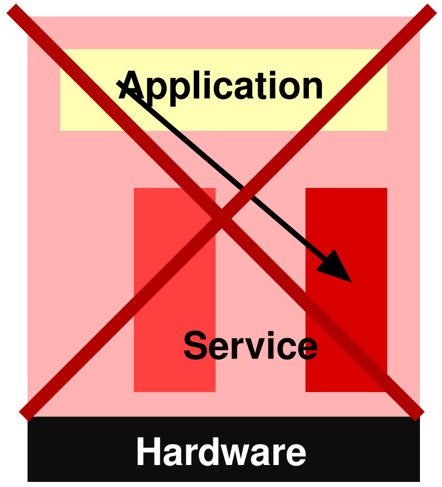

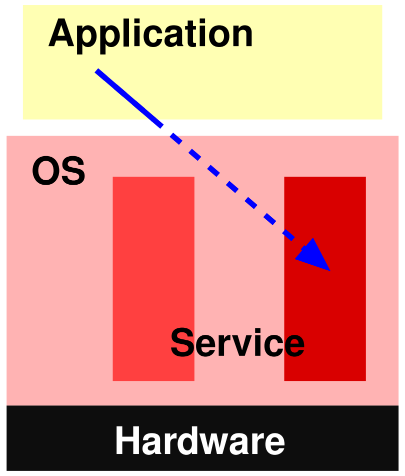

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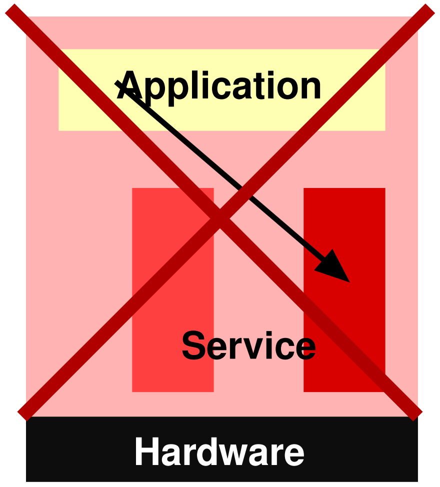

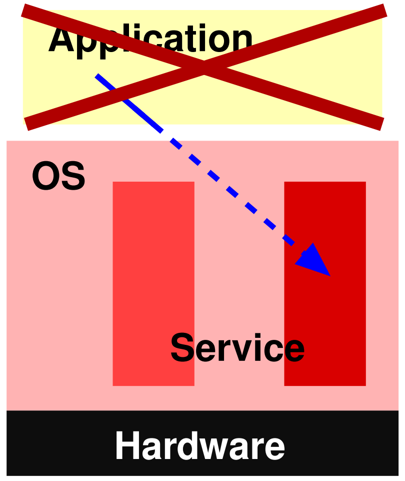

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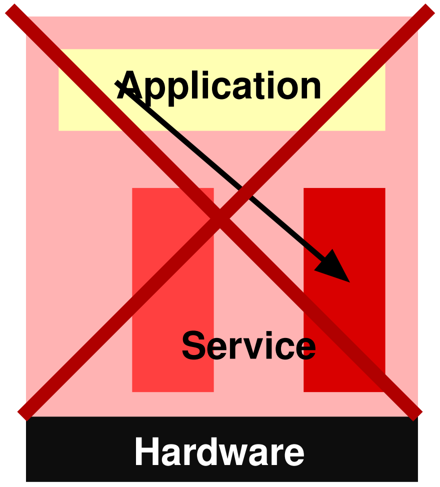

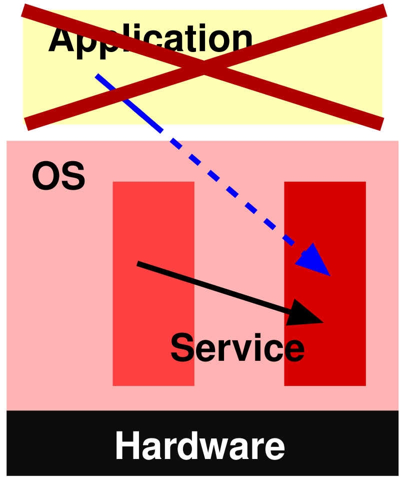

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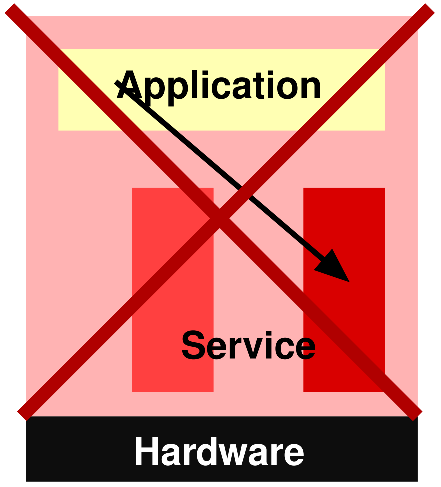

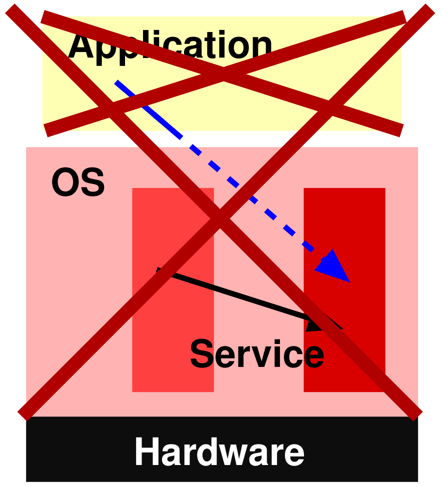

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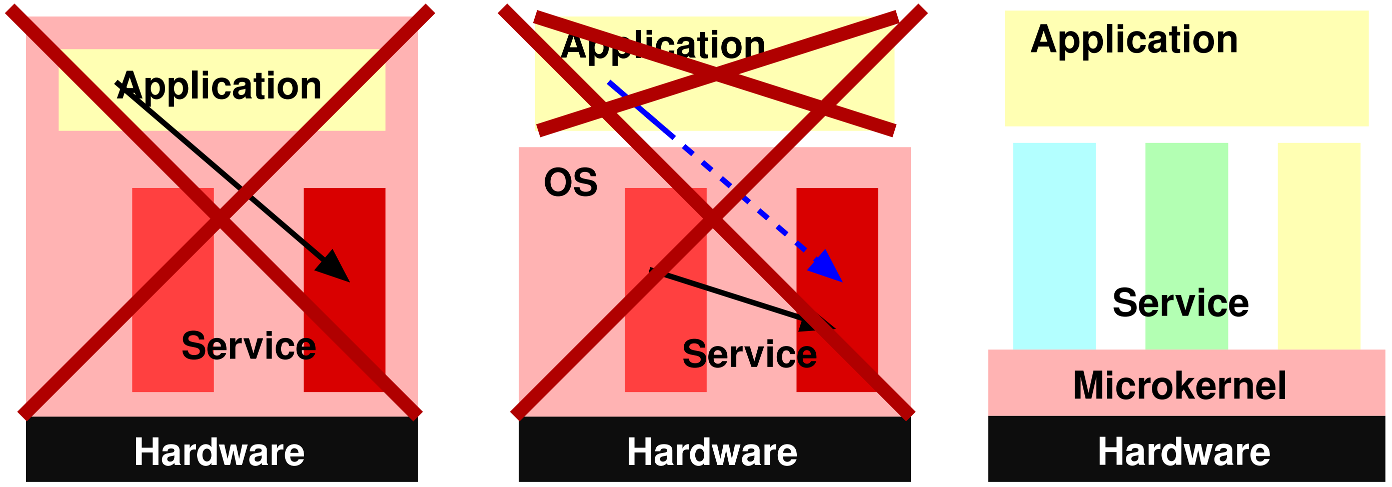

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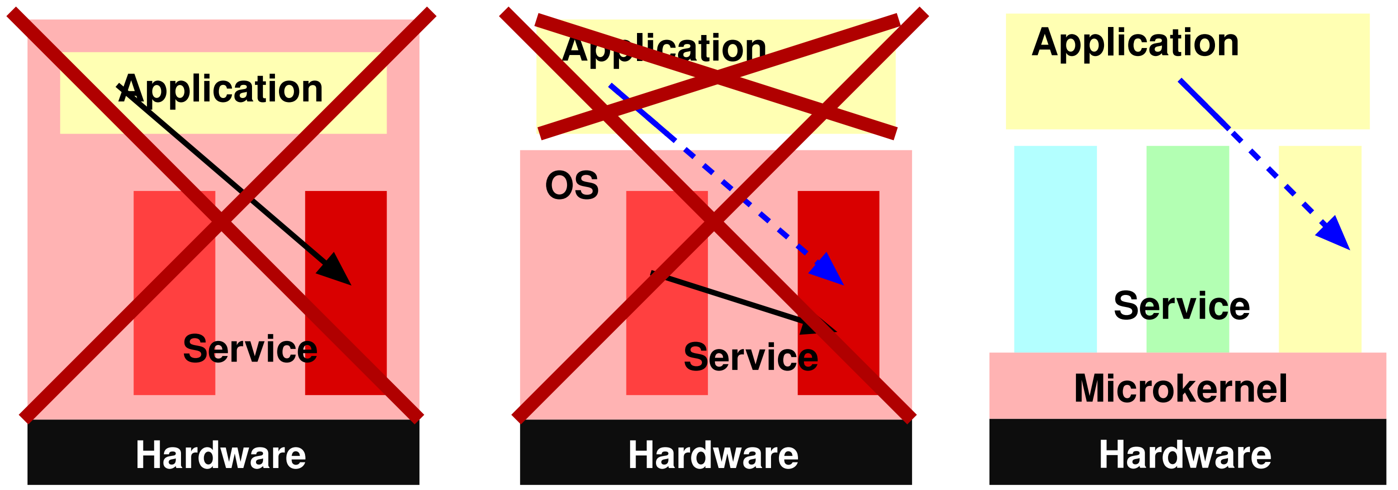

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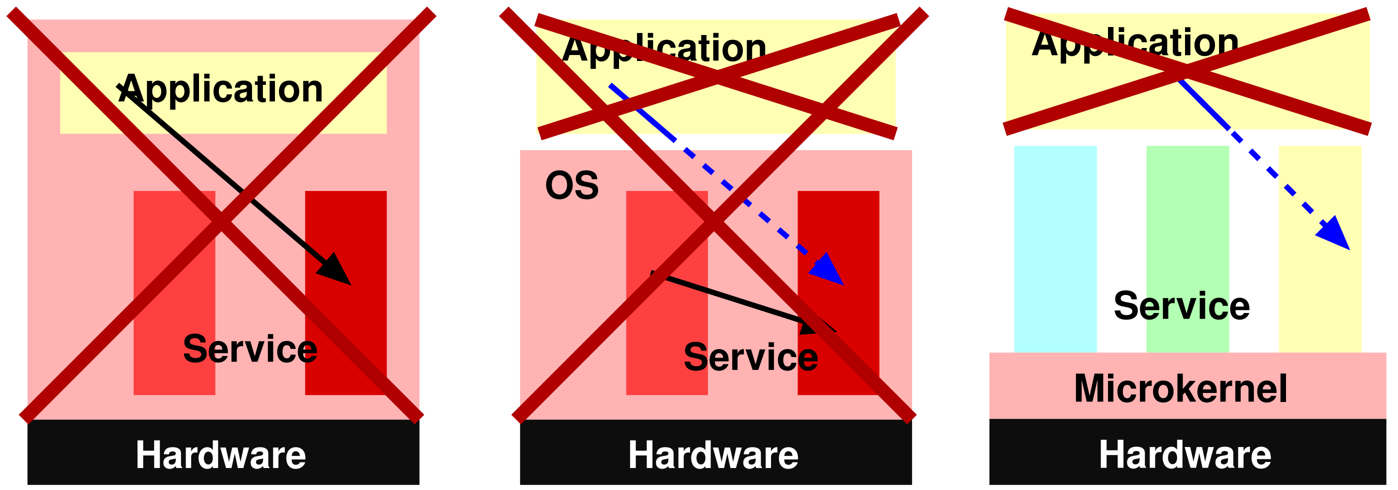

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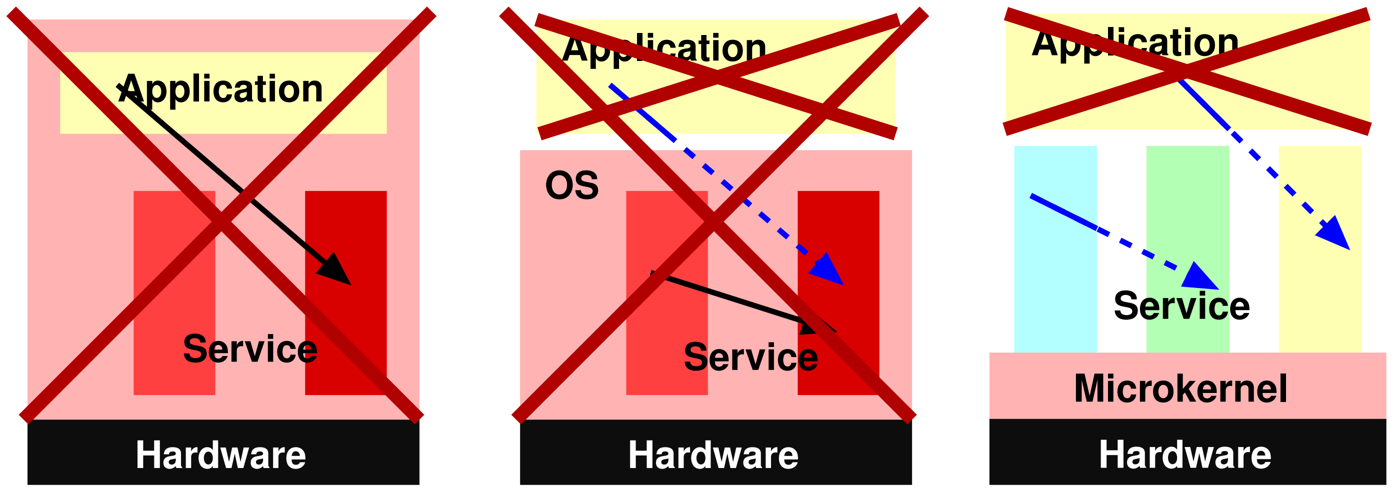

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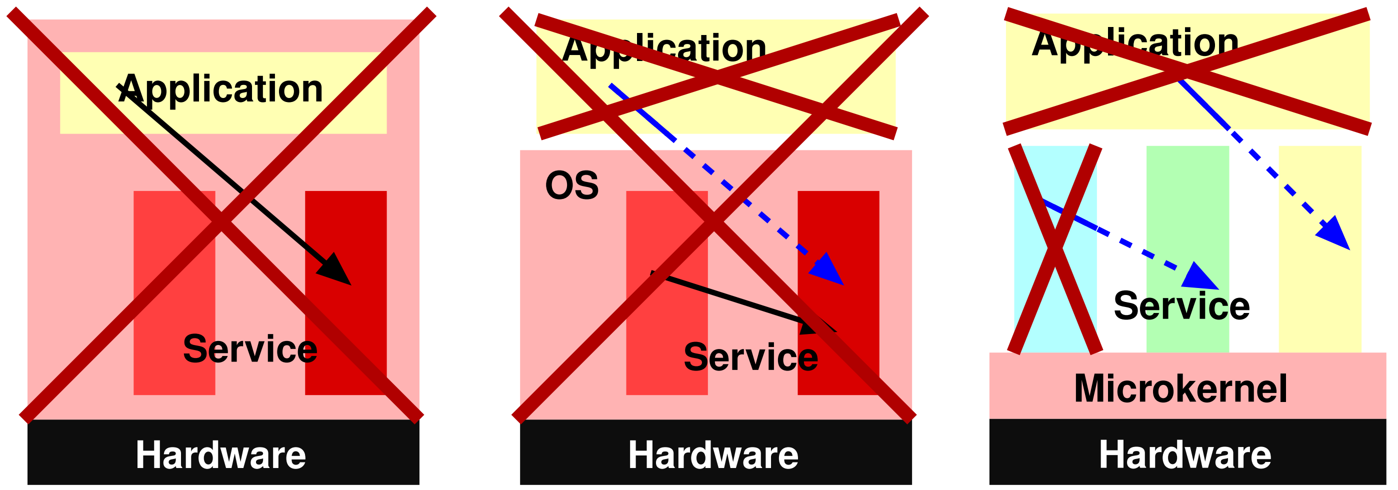

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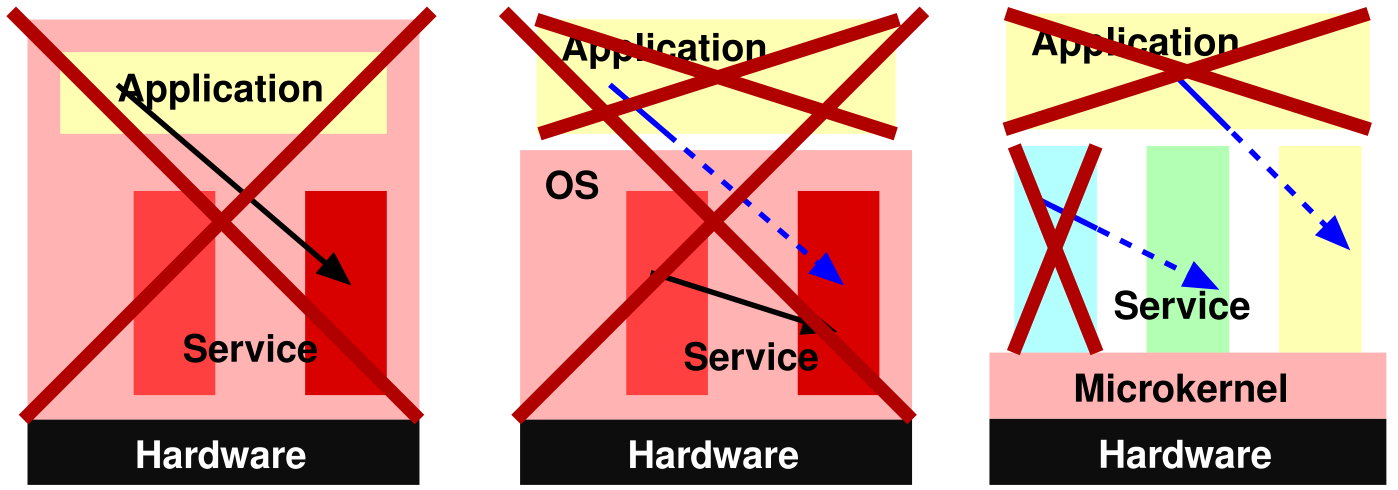

System:	traditional embedded	Linux/ Windows	Microkernel-based
TCB:	**all** code	100,000’s loc	10,000’s loc

MICROKERNEL PROMISES

- Combat kernel complexity, increase robustness, maintainability
  - ➜ dramatic reduction of amount of privileged code
  - ➜ modularisation with hardware-enforced interfaces
  - ➜ normal resource management applicable to system services
- Flexibility, adaptability, extensibility
  - ➜ policies defined at user level, easy to change
  - ➜ additional services provided by adding servers
- Hardware abstraction
  - ➜ hardware-dependent part of system is small, easy to optimise
- Security, safety
  - ➜ internal protection boundaries

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slow, inflexible

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100μsec IPC

IPC Costs

- First-generation microkernels
  - ➜ Mach, Chorus, Amoeba

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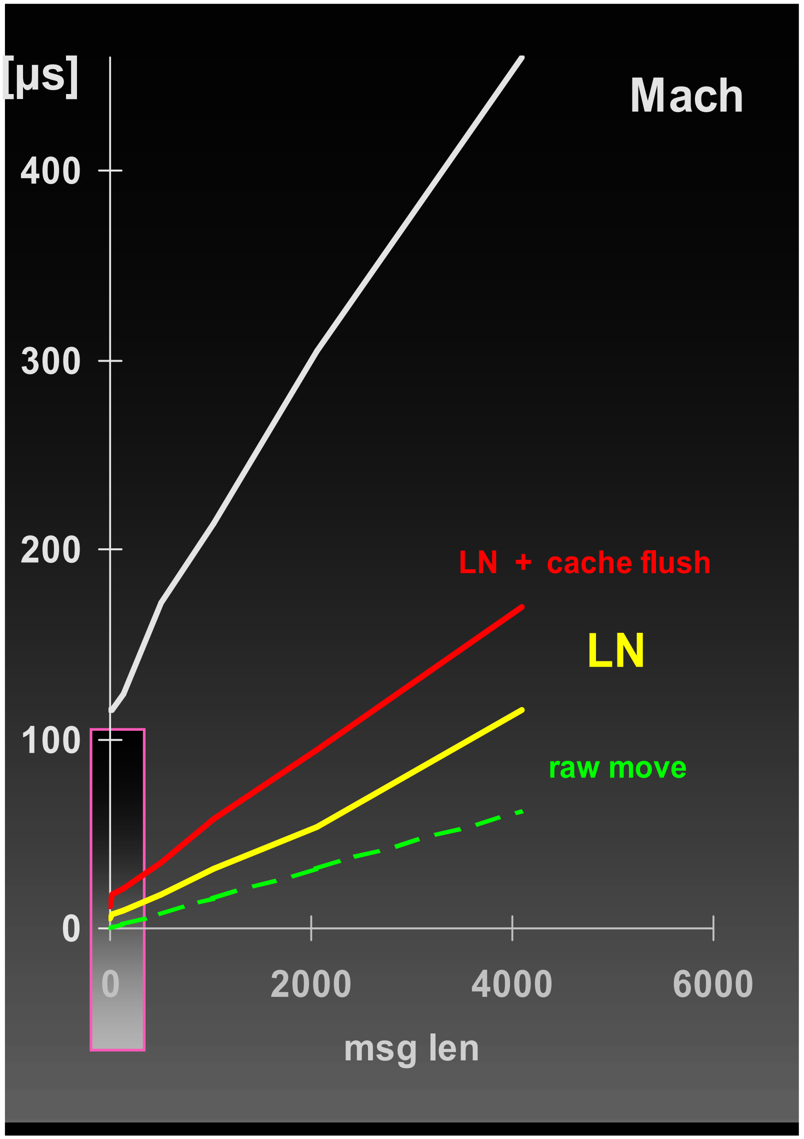
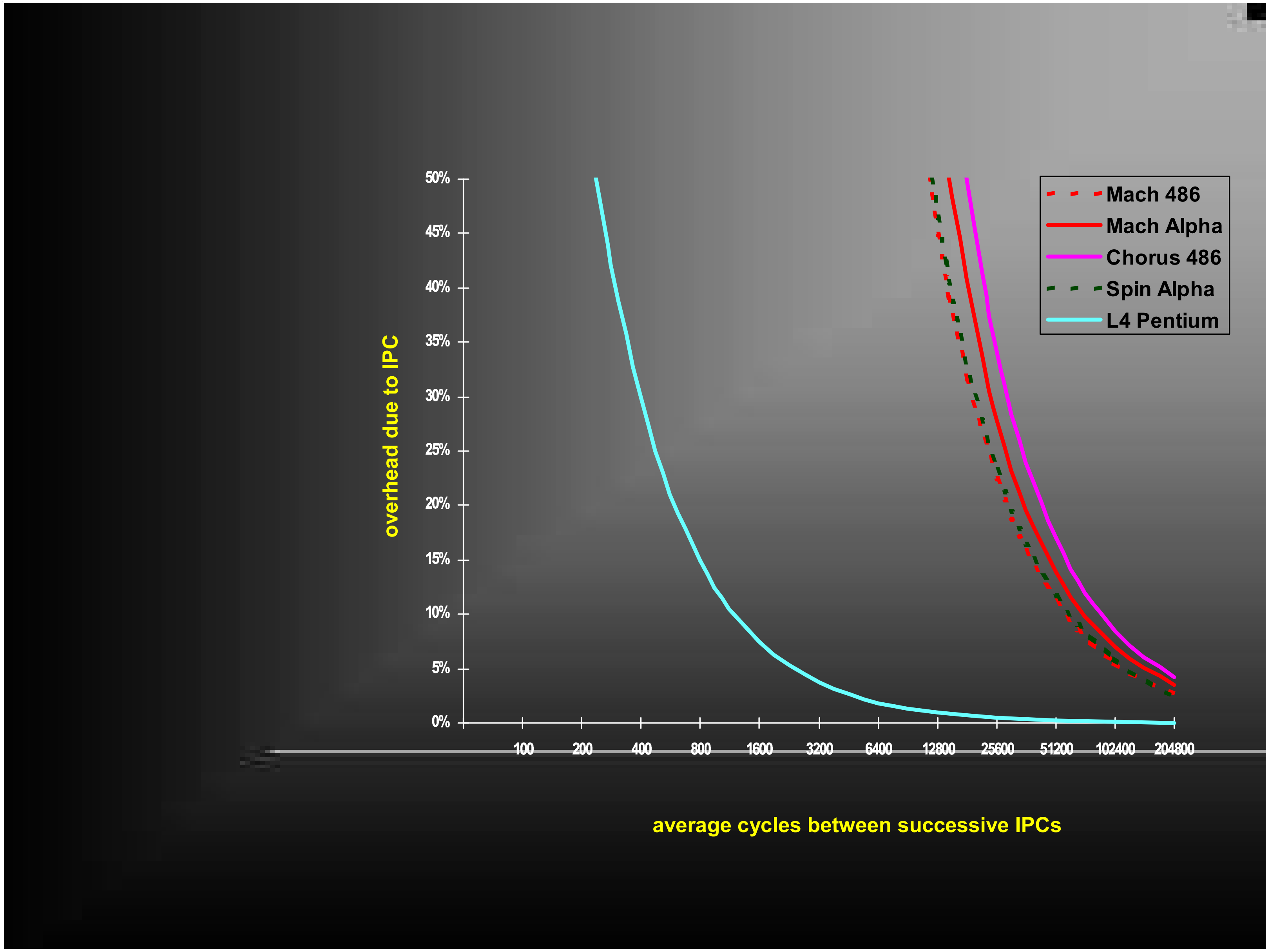
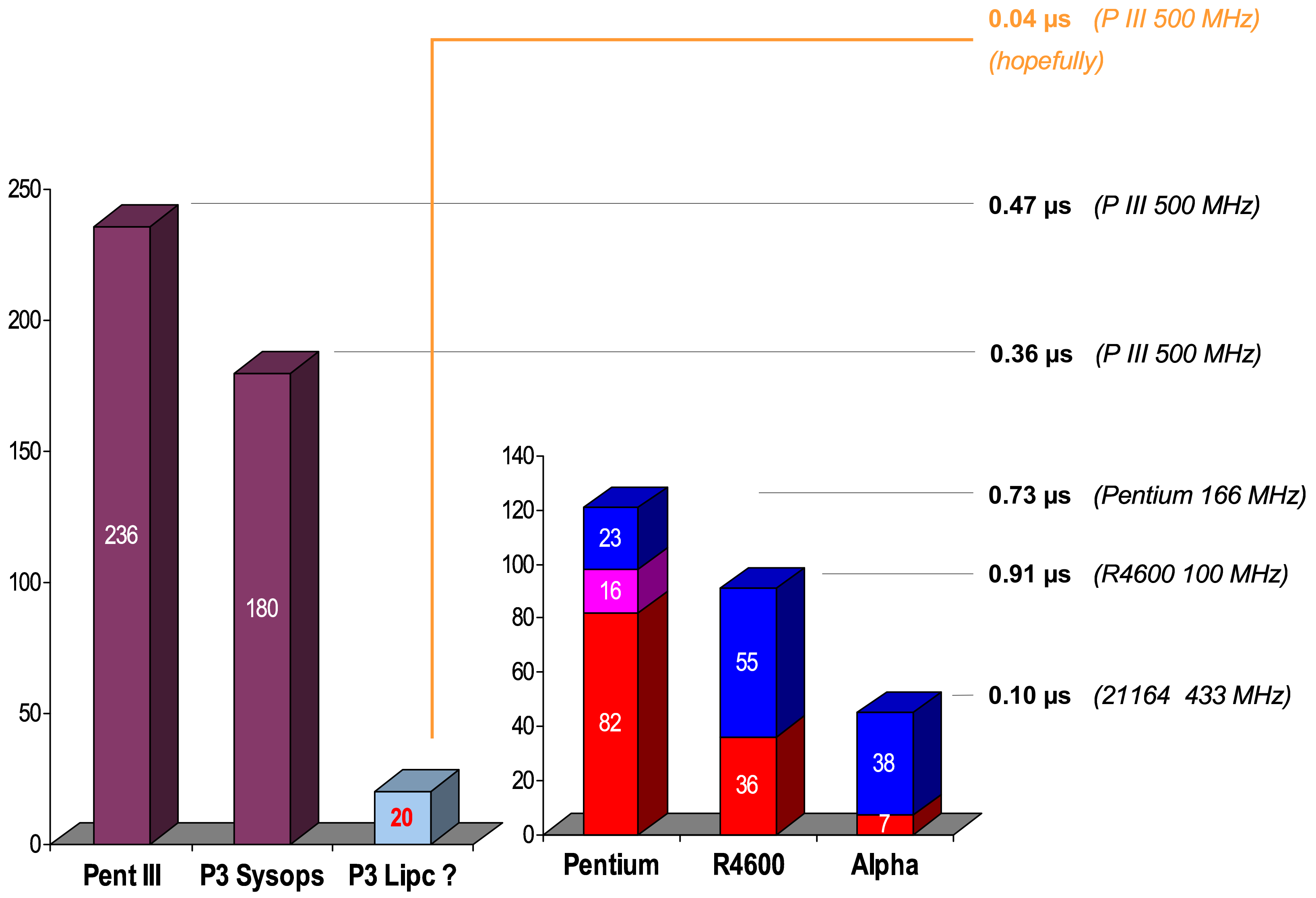
- L4 does better
  - ➜ close to hardware cost
  - ➜ 20 times faster than Mach on identical hardware



IPC Cost Implications



L4 IPC



0.04 µs (P III 500 MHz) (hopefully)
0.47 µs (P III 500 MHz)
0.36 µs (P III 500 MHz)
0.73 µs (Pentium 166 MHz)
0.91 µs (R4600 100 MHz)
0.10 µs (21164 433 MHz)
250
200
150
100
50
0
236
180
20
Pent III
P3 Sysops
P3 Lipc ?
140
120
100
80
60
40
20
0
23
16
82
55
36
38
7
Pentium
R4600
Alpha

MICROKERNEL PERFORMANCE

FIRST-GENERATION MICROKERNELS WERE SLOW

- Reasons: Poor design [Liedtke SOSP 95]
  - ➜ complex API
  - ➜ too many features
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- L4 is fast due to small cache footprint
  - ➜ 10–14 I-cache lines
  - ➜ 8 D-cache lines
  - ➜ small cache footprint $\Rightarrow$ CPU limited

WHAT MAKES A MICROKERNEL FAST?

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  - ➜ minimality: no unnecessary features
  - ➜ orthogonality: complementary features
  - ➜ well-designed, and *well implemented* from scratch!

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- Design principle (minimality):

  A feature is only allowed in the kernel if this is required for the implementation of a secure system.

L4 History

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- Original version by Jochen Liedtke (GMD) $\approx$ 93–95
  - ➜ “Version 2” API
  - ➜ i486 assembler
  - ➜ IPC 20 times faster than Mach [SOSP 93, 95]

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  - ➜ "Version 2" API
  - ➜ i486 assembler
  - ➜ IPC 20 times faster than Mach [SOSP 93, 95]
- Other L4 V2 implementations:
  - ➜ L4/MIPS64: assembler + C (UNSW) 95–97
    - ➜ fastest kernel on single-issue CPU (100 cycles)
  - ➜ L4/Alpha: PAL + C (Dresden/UNSW), 95–97
    - ➜ first released SMP version
  - ➜ Fiasco (Pentium): C++ (Dresden), 97–99

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- Implementations
  - ➜ Pentium: assembler, Liedtke (IBM), 97-98
  - ➜ *Hazelnut* (Pentium+ARM), C, Liedtke et al (Karlsruhe), 98–99

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- Portable kernel:
  - ➜ $\approx$ 3 person months for core functionality
  - ➜ 6–12 person months for full functionality & optimisation

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  - ➜ transitional API (pre-seL4)
  - ➜ de-featured (timeouts, “long” IPC, recursive mappings)
  - ➜ reduced memory footprint for embedded systems

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- You’ll be using the (unreleased) N2 API implementation

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- NICTA L4-embedded commercially deployed
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  - ➜ under evaluation/development for other products at a number of multinationals
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  - ➜ about to establish strong presence in wireless and CE markets
- NICTA spinning out Open Kernel Labs
  - ➜ further development of L4-embedded
  - ➜ professional services for L4 users
  - ➜ commercialisation of present NICTA microkernel research

L4 Future

- Security API: NICTA seL4
  - ➜ draft published March 06
  - ➜ semi-formal specification in Haskell
  - ➜ “executable spec”: Haskell implementation plus ISA simulator
  - ➜ used for exercising and porting apps
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- Formal verification of L4 implementation: L4.verified project
  - ➜ mathematical proof that implementation matches spec

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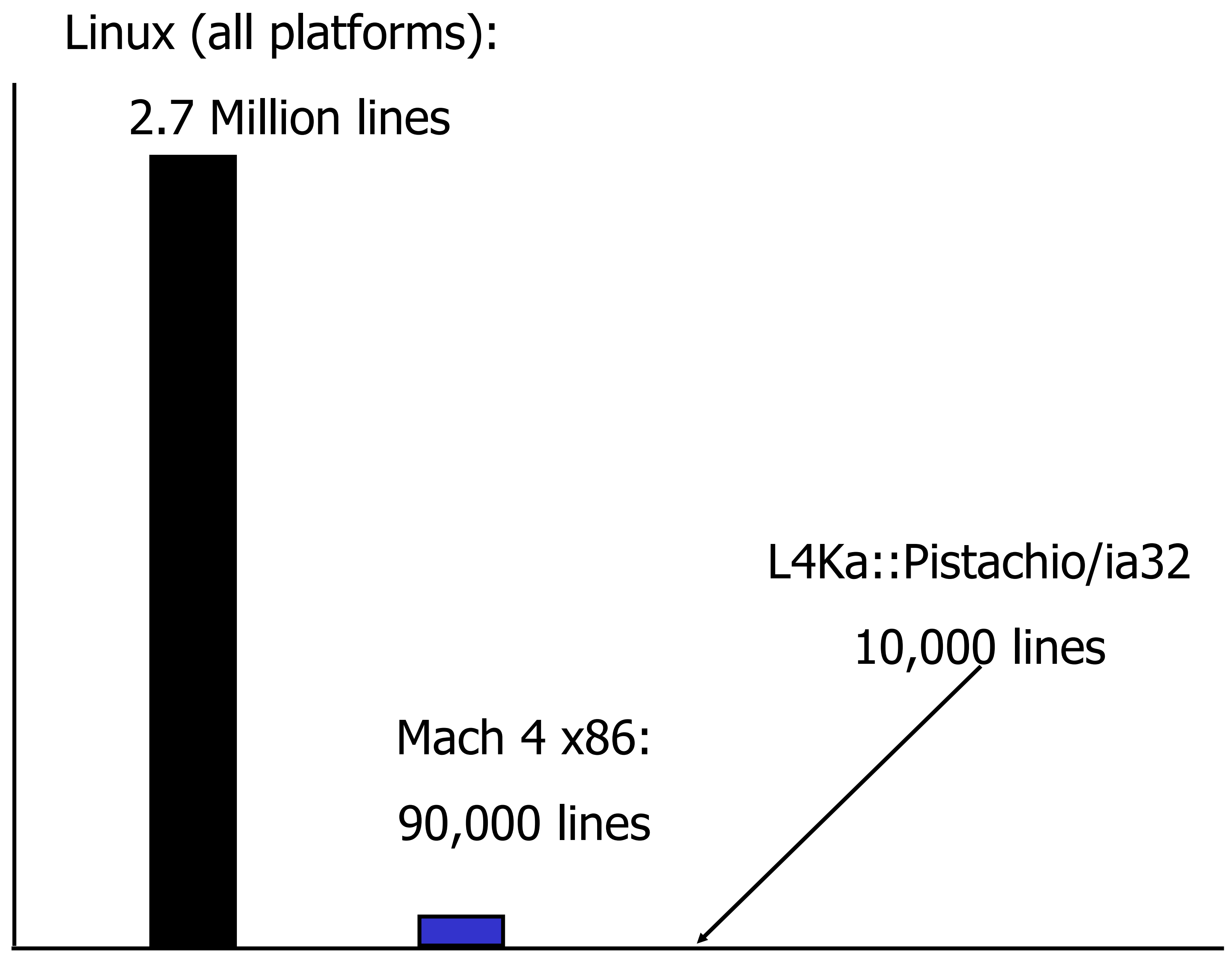
Size Comparison



PISTACHIO PERFORMANCE: IPC

	port/	C++		optimised	
Architecture	**optimisation**	**intra AS**	**inter AS**	**intra AS**	**inter AS**
Pentium-3	UKa	180	367	113	305
Small Spaces	UKa				213
Pentium-4	UKa	385	983	196	416
Itanium 2	UKa/NICTA	508	508	36	36
cross CPU	UKa	7419	7410	N/A	N/A
MIPS64	NICTA/UNSW	276	276	109	109
cross CPU	NICTA/UNSW	3238	3238	690	690
PowerPC-64	NICTA/UNSW	330	518	200‡	200‡
Alpha 21264	NICTA/UNSW	440	642	≈70†	≈70†
ARM/XScale	NICTA/UNSW	340	340	151	151

† “Version 2” assembler kernel

‡ Guestimate!

L4 Abstractions and Mechanisms

Three basic abstractions:

- Address spaces
- Threads
- Time (second-class abstraction in N2 API, to vanish completely)

Two basic mechanisms:

- Inter-process communication (IPC)
- Mapping

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  - ➜ initially empty
  - ➜ populated by mapping in frames
- Mapping performed by privileged MapControl() syscall
  - ➜ can only be called from *root task*
  - ➜ also used for revoking mappings (unmap operation)
- Root task
  - ➜ initial address space created at boot time
  - ➜ controls system resources
  - ➜ non-delegatable privilege (shortcoming of N2 API)

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  - ➜ creation, destruction, association with address space

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  - ➜ thread-ID is unique identifier
- Threads managed by user-level servers
  - ➜ creation, destruction, association with address space
- Thread attributes:
  - ➜ scheduling parameters (time slice, priority)
  - ➜ unique ID
  - ➜ address space
  - ➜ page-fault and exception handler

L4 Abstractions: Time

- Used for scheduling time slices
  - ➜ thread has fixed-length time slice for preemption
  - ➜ time slices allocated from (finite or infinite) time quantum
    - ➜ notification when exceeded
- In earlier L4 versions also used for IPC timeouts
  - ➜ removed in N2

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- Synchronous message-passing operation
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  - ➜ short messages passed in registers
- Can be blocking or polling (fail if partner not ready)
- Asynchronous notification variant
  - ➜ no data transfer, only sets notification bit in receiver
  - ➜ receiver can wait (block) or poll

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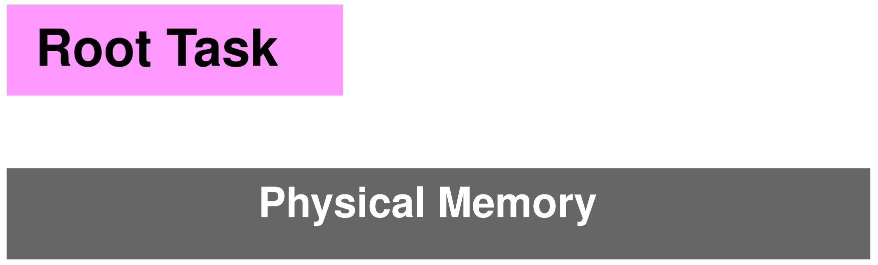

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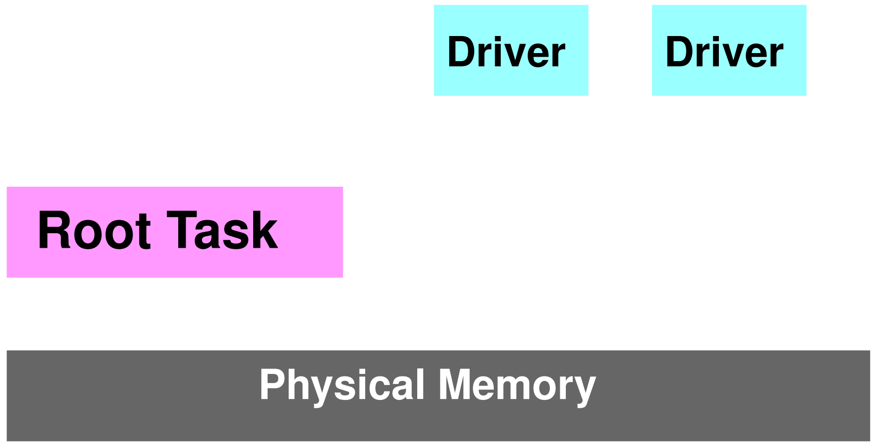

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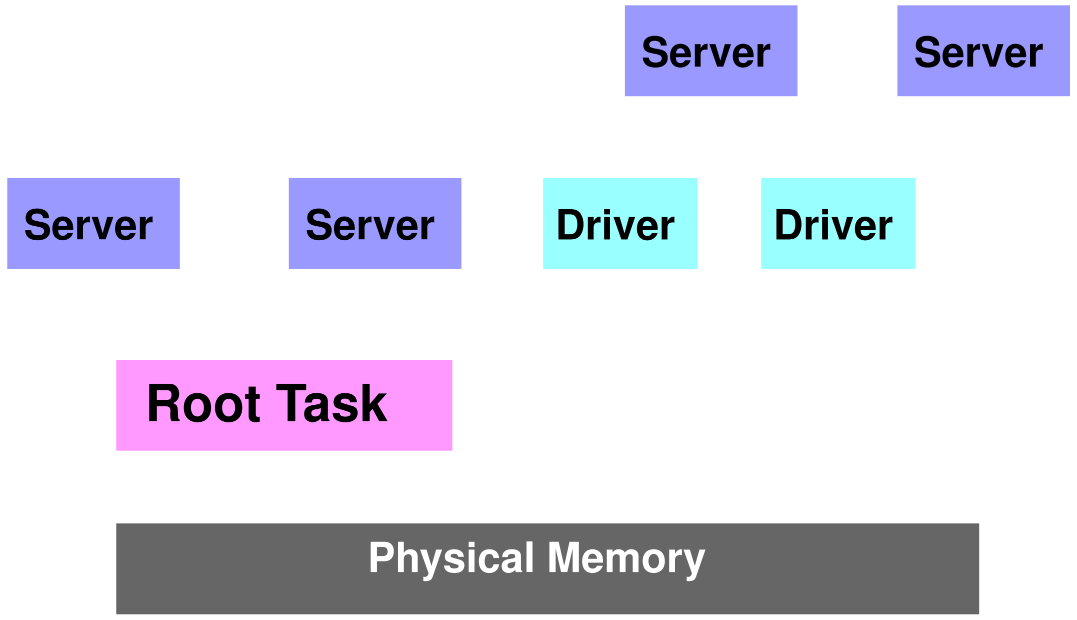

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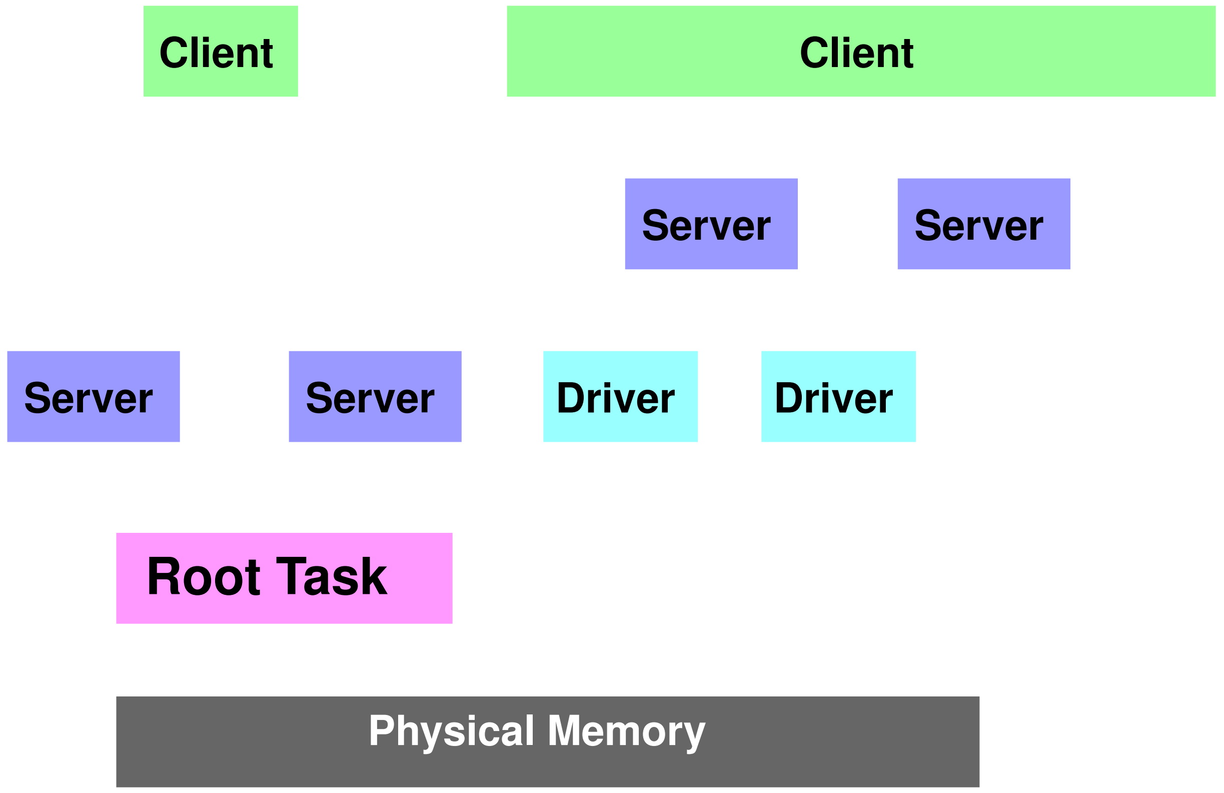

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  - ➜ kernel fakes IPC message from exceptor thread to its exception handler
  - ➜ exception handler may reply with message specifying new IP, SP
  - ➜ can be signal handler, emulation code, stub for IPCing to server, ...

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- Device drivers

  ➜ user-level threads registered for interrupt IPC
  ➜ map device registers