High-Level Synthesis for FPGAs: From Prototyping to Deployment

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***Abstract*—Escalating system-on-chip design complexity is pushing the design community to raise the level of abstraction beyond register transfer level. Despite the unsuccessful adoptions of early generations of commercial high-level synthesis (HLS) systems, we believe that the tipping point for transitioning to HLS methodology is happening now, especially for field-programmable gate array (FPGA) designs. The latest generation of HLS tools has made significant progress in providing wide language coverage and robust compilation technology, platform-based modeling, advancement in core HLS algorithms, and a domain-specific approach. In this paper, we use AutoESL's AutoPilot HLS tool coupled with domain-specific system-level implementation platforms developed by Xilinx as an example to demonstrate the effectiveness of state-of-art C-to-FPGA synthesis solutions targeting multiple application domains. Complex industrial designs targeting Xilinx FPGAs are also presented as case studies, including comparison of HLS solutions versus optimized manual designs. In particular, the experiment on a sphere decoder shows that the HLS solution can achieve an 11–31% reduction in FPGA resource usage with improved design productivity compared to hand-coded design.**

***Index Terms*—Domain-specific design, field-programmable gate array (FPGA), high-level synthesis (HLS), quality of results (QoR).**

I. Introduction

THE RAPID INCREASE of complexity in system-on-a-chip (SoC) design has encouraged the design community to seek design abstractions with better productivity than register transfer level (RTL). Electronic system-level (ESL) design automation has been widely identified as the next productivity boost for the semiconductor industry, where high-level synthesis (HLS) plays a central role, enabling the automatic synthesis of high-level, untimed or partially timed specifications (such as in C or SystemC) to low-level cycle-accurate RTL specifications for efficient implementation in application-specific integrated circuits (ASICs) or field-programmable gate arrays (FPGAs). This synthesis can be optimized taking into account the performance, power, and cost requirements of a particular system.

Despite the past failure of the early generations of commercial HLS systems (started in the 1990s), we see a rapidly growing demand for innovative, high-quality HLS solutions for the following reasons.

1) *Embedded processors are in almost every SoC*: With the coexistence of micro-processors, digital signal processors (DSPs), memories and custom logic on a single chip, more software elements are involved in the process of designing a modern embedded system. An automated HLS flow allows designers to specify design functionality in high-level programming languages such as C/C++ for both embedded software and customized hardware logic on the SoC. This way, they can quickly experiment with different hardware/software boundaries and explore various area/power/performance tradeoffs from a single common functional specification.
2) *Huge Silicon capacity requires a higher level of abstraction*: Design abstraction is one of the most effective methods for controlling complexity and improving design productivity. For example, the study from NEC [91] shows that a 1M-gate design typically requires about 300K lines of RTL code, which cannot be easily handled by a human designer. However, the code density can be easily reduced by 7X–10X when moved to high-level specification in C, C++, or SystemC. In this case, the same 1M-gate design can be described in 30K–40K lines of behavioral description, resulting in a much reduced design complexity.
3) *Behavioral IP reuse improves design productivity*: In addition to the line-count reduction in design specifications, behavioral synthesis has the added value of allowing efficient reuse of behavioral intellectual properties (IPs). As opposed to RTL IP which has fixed microarchitecture and interface protocols, behavioral IP can be retargeted to different implementation technologies or system requirements.
4) *Verification drives the acceptance of high-level specification*: Transaction-level modeling (TLM) with SystemC [109] or similar C/C++ based extensions has become a

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very popular approach to system-level verification [36]. Designers commonly use SystemC TLMs to describe virtual software/hardware platforms, which serve three important purposes: early embedded software development, architectural modeling and exploration, and functional verification. The wide availability of SystemC functional models directly drives the need for SystemC-based HLS solutions, which can automatically generate RTL code through a series of formal constructive transformations. This avoids slow and error-prone manual RTL re-coding, which is the standard practice in the industry today.

5) *Trend toward extensive use of accelerators and heterogeneous SoCs*: Many SoCs, or even chip multiprocessors move toward inclusion of many accelerators (or algorithmic blocks), which are built with custom architectures, largely to reduce power compared to using multiple programmable processors. According to ITRS prediction [111], the number of on-chip accelerators will reach 3000 by 2024. In FPGAs, custom architectures for algorithmic blocks provide higher performance in a given amount of resources than synthesized soft processors. These algorithmic blocks are particularly appropriate for HLS.

Although these reasons for adopting HLS design methodology are common to both ASIC and FPGA designers, we also see additional forces that push the FPGA designers for faster adoption of HLS tools.

1) *Less pressure for formal verification*: The ASIC manufacturing cost in nanometer integrated circuit (IC) technologies is well over $1M [111]. There is tremendous pressure for the ASIC designers to achieve first tape-out success. Yet formal verification tools for HLS are not mature, and simulation coverage can be limited for multimillion gate SoC designs. This is a significant barrier for HLS adoption in the ASIC world. However, for FPGA designs, in-system simulation is possible with much wider simulation coverage. Design iterations can be done quickly and inexpensively without huge manufacturing costs.
2) *Ideal for platform-based synthesis*: Modern FPGAs embed many predefined/fabricated IP components, such as arithmetic function units, embedded memories, embedded processors, and embedded system buses. These predefined building blocks can be modeled precisely ahead of time for each FPGA platform and, to a large extent, confine the design space. As a result, it is possible for modern HLS tools to apply a platform-based design methodology [52] and achieve higher quality of results (QoR).
3) *More pressure for time-to-market*: FPGA platforms are often selected for systems where time-to-market is critical, in order to avoid long chip design and manufacturing cycles. Hence, designers may accept increased performance, power, or cost in order to reduce design time. As shown in Section IX, modern HLS tools put this tradeoff in the hands of a designer allowing significant reduction in design time or, with additional effort, QoR comparable to hand-written RTL.
4) *Accelerated or reconfigurable computing calls for C/C++ based compilation/synthesis to FPGAs*: Recent advances in FPGAs have made reconfigurable computing platforms feasible to accelerate many high-performance computing (HPC) applications, such as image and video processing, financial analytics, bioinformatics, and scientific computing applications. Since RTL programming in VHDL or Verilog is unacceptable to most application software developers, it is essential to provide a highly automated compilation/synthesis flow from C/C++ to FPGAs.

As a result, a growing number of FPGA designs are produced using HLS tools. Some example application domains include 3 G/4 G wireless systems [39], [82], aerospace applications [76], image processing [28], lithography simulation [13], and cosmology data analysis [53]. Xilinx is also in the process of incorporating HLS solutions in their Video Development Kit [118] and DSP Develop Kit [98] for all Xilinx customers.

This paper discusses the reasons behind the recent success in deploying HLS solutions to the FPGA community. In Section II, we review the evolution of HLS systems and summarize the key lessons learned. In Sections III–VIII, using a state-of-art HLS tool as an example, we discuss some key reasons for the wider adoption of HLS solutions in the FPGA design community, including wide language coverage and robust compilation technology, platform-based modeling, advancement in core HLS algorithms, improvements on simulation and verification flow, and the availability of domain-specific design templates. Then, in Section IX, we present the HLS results on several real-life industrial designs and compare with manual RTL implementations. Finally, in Section X, we conclude this paper with discussions of future challenges and opportunities.

II. Evolution of HLS for FPGA

In this section we briefly review the evolution of HLS by looking at representative tools. Compilers for high-level languages have been successful in practice since the 1950s. The idea of automatically generating circuit implementations from high-level behavioral specifications arises naturally with the increasing design complexity of ICs. Early efforts (in the 1980s and early-1990s) on HLS were mostly research projects, where multiple prototype tools were developed to call attention to the methodology and to experiment with various algorithms. Most of those tools, however, made rather simplistic assumptions about the target platform and were not widely used. Early commercialization efforts in the 1990s and early-2000s attracted considerable interest among designers, but also failed to gain wide adoption, due in part to usability issues and poor QoRs. More recent efforts in HLS have improved usability by increasing input language coverage and platform integration, as well as improving QoRs.

A. Early Efforts

Since the history of HLS is considerably longer than that of FPGAs, most early HLS tools targeted ASIC designs.

A pioneering HLS tool, Carnegie-Mellon University design automation (CMU-DA), was built by researchers at Carnegie Mellon University in the 1970s [30], [72]. In this tool, the design is specified at behavior level using the instruction set processor specification (ISPS) language [4]. It is then translated into an intermediate data-flow representation called the Value Trace [80] before producing RTL. Many common code-transformation techniques in software compilers, including dead-code elimination, constant propagation, redundant sub-expression elimination, code motion, and common sub-expression extraction could be performed. The synthesis engine also included many steps familiar in hardware synthesis, such as datapath allocation, module selection, and controller generation. CMU-DA also supported hierarchical design and included a simulator of the original ISPS language. Although many of the methods used were very preliminary, the innovative flow and the design of toolsets in CMU-DA quickly generated considerable research interest.

In the subsequent years in the 1980s and early-1990s, a number of similar HLS tools were built, mostly for research and prototyping. Examples of academic efforts include ADAM [38], [47], HAL [73], MIMOLA [63], Hercules/Hebe [25], [26], [56], and Hyper/Hyper-LP [10], [78]. Industry efforts include Cathedral and its successors [27], Yorktown Silicon Compiler [11], and BSSC [93], among many others. Like CMU-DA, these tools typically decompose the synthesis task into a few steps, including code transformation, module selection, operation scheduling, datapath allocation, and controller generation. Many fundamental algorithms addressing these individual problems were also developed. For example, the list scheduling algorithm [1] and its variants are widely used to solve scheduling problems with resource constraints [71]; the force-directed scheduling algorithm developed in HAL [74] is able to optimize resource requirements under a performance constraint. The path-based scheduling algorithm in the Yorktown Silicon Compiler is useful to optimize performance with conditional branches [12]. The Sehwa tool in ADAM is able to generate pipelined implementations and explore the design space by generating multiple solutions [48], [70]. The relative scheduling technique developed in Hebe is an elegant way to handle operations with unbounded delay [57]. Conflict-graph coloring techniques were developed and used in several systems to share resources in the datapath [58], [73].

These early high-level tools often used custom languages for design specification. Besides the ISPS language used in CMU-DA, a few other languages were notable. HardwareC is a language designed for use in the Hercules system [55]. Based on the popular C programming language, it supports both procedural and declarative semantics and has built-in mechanisms to support design constraints and interface specifications. This is one of the earliest C-based hardware synthesis languages for HLS. It is interesting to compare it with similar languages later. The Silage language used in Cathedral/Cathedral-II was specifically designed for the synthesis of digital signal processing hardware [27]. It has built-in support for customized data types, and allows easy transformations [10], [78]. The Silage language, along with the Cathedral-II tool, represented an early domain-specific approach in HLS.

These early research projects helped to create a basis for algorithmic synthesis with many innovations, and some were even used to produce real chips. However, these efforts did not lead to wide adoption among designers. A major reason is that the methodology of using RTL synthesis was not yet widely accepted at that time and RTL synthesis tools were not mature. Thus, HLS, built on top of RTL synthesis, did not have a sound foundation in practice. In addition, simplistic assumptions were often made in these early systems—many of them were "technology independent" (such as Olympus), and inevitably led to suboptimal results.

With improvements in RTL synthesis tools and the wide adoption of RTL-based design flows in the 1990s, industrial deployment of HLS tools became more practical. Proprietary tools were built in major semiconductor design houses including IBM [5], Motorola [59], Philips [62], and Siemens [6]. Major EDA vendors also began to provide commercial HLS tools. In 1995, Synopsys announced Behavioral Compiler [89], which generates RTL implementations from behavioral hardware description language (HDL) code and connects to downstream tools. Similar tools include Monet from Mentor Graphics [34] and Visual Architect from Cadence [44]. These tools received wide attention, but failed to widely replace RTL design. This is partly ascribed to the use of behavioral HDLs as input languages, which are not popular among algorithm and system designers and require steep learning curves.

B. Recent Efforts

Since 2000, a new generation of HLS tools has been developed in both academia and industry. Unlike many predecessors, most of these tools focus on using C/C++ or C-like languages to capture design intent. This makes the tools much more accessible to algorithm and system designers compared to previous tools that only accept HDL languages. It also enables hardware and software to be built using a common model, facilitating software/hardware co-design and co-verification. The use of C-based languages also makes it easy to leverage the newest technologies in software compilers for parallelization and optimization in the synthesis tools.

In fact, there has been an ongoing debate on whether C-based languages are proper choices for HLS [32], [79]. Despite the many advantages of using C-based languages, opponents often criticize C/C++ as languages only suitable for describing sequential software that runs on microprocessors. Specifically, the deficiencies of C/C++ include the following.

1) Standard C/C++ lack built-in constructs to explicitly specify bit accuracy, timing, concurrency, synchronization, hierarchy, and others, which are critical to hardware design.
2) C and C++ have complex language constructs, such as pointers, dynamic memory management, recursion, and polymorphism, which do have efficient hardware counterparts and lead to difficulty in synthesis.

To address these deficiencies, modern C-based HLS tools have introduced additional language extensions and restrictions to make C inputs more amenable to hardware synthesis. Common approaches include both restriction to a synthesizable subset

that discourages or disallows the use of dynamic constructs (as required by most tools) and introduction of hardware-oriented language extensions (HardwareC [55], SpecC [35], Handel-C [96]), libraries (SystemC [109]), and compiler directives to specify concurrency, timing, and other constraints. For example, Handel-C allows the user to specify clock boundaries explicitly in the source code. Clock edges and events can also be explicitly specified in SpecC and SystemC. Pragmas and directives along with a subset of ANSI C/C++ are used in many commercial tools. An advantage of this approach is that the input program can be compiled using standard C/C++ compilers without change, so that such a program or a module of it can be easily moved between software and hardware and co-simulation of hardware and software can be performed without code rewriting. At present, most commercial HLS tools use some form of C-based design entry, although tools using other input languages (e.g., BlueSpec [103], Esterel [31], and MATLAB [43]) also exist.

Another notable difference between the new generation of HLS tools and their predecessors is that many tools are built targeting implementation on FPGA. FPGAs have continually improved in capacity and speed in recent years, and their programmability makes them an attractive platform for many applications in signal processing, communication, and HPC. There has been a strong desire to make FPGA programming easier, and many HLS tools are designed to specifically target FPGAs, including ASC [65], CASH [9], C2H [99], DIME-C [114], GAUT [23], Handel-C Compiler (now part of Mentor Graphics DK Design Suite) [96], Impulse C [75], ROCCC [88], [40], SPARK [41], [42], Streams-C [37], and Trident [83], [84]. ASIC tools also commonly provide support for targeting an FPGA tool flow in order to enable system emulation.

Among these HLS tools, many are designed to focus on a specific application domain. For example, the Trident Compiler, developed at Los Alamos National Lab, Los Alamos, NM, is an open-source tool focusing on the implementation of floating-point scientific computing applications on FPGA. Many others, including GAUT, Streams-C, ROCCC, ASC, and Impulse C, target streaming DSP applications. Following the tradition of Cathedral, these tools implement architectures consisting of a number of modules connected using first-in first-out (FIFO) channels. Such architectures can be integrated either as a standalone DSP pipeline, or integrated to accelerate code running on a processor (as in ROCCC).

As of 2010, major commercial C-based HLS tools include AutoESL's AutoPilot [95] (originated from UCLA xPilot project [17]), Cadence's C-to-Silicon Compiler [3], [104], Forte's Cynthesizer [66], Mentor's Catapult C [7], NEC's Cyber Workbench [90], [92], and Synopsys Synphony C [117] (formerly, Synfora's PICO Express, originated from a long-range research effort in HP Labs [50]).

C. Lessons Learned

Despite extensive development efforts, most commercial HLS efforts have failed. We summarize reasons for past failures as follows.

1) *Lack of Comprehensive Design Language Support:* The first generation of the HLS synthesis tools could not synthesize high-level programming languages. Instead, untimed or partially timed behavioral HDL was used. Such design entry marginally raised the abstraction level, while imposing a steep learning curve on both software and hardware developers.

Although early C-based HLS technologies have considerably improved the ease of use and the level of design abstraction, many C-based tools still have glaring deficiencies. For instance, C and C++ lack the necessary constructs and semantics to represent hardware attributes such as design hierarchy, timing, synchronization, and explicit concurrency. SystemC, on the contrary, is ideal for system-level specification with software/hardware co-design. However, it is foreign to algorithmic designers and has slow simulation speed compared to pure ANSI C/C++ descriptions. Unfortunately, most early HLS solutions commit to only one of these input languages, restricting their usage to niche application domains.

2) *Lack of Reusable and Portable Design Specification:* Many HLS tools have required users to embed detailed timing and interface information as well as the synthesis constraints into the source code. As a result, the functional specification became highly tool-dependent, target-dependent, and/or implementation-platform dependent. Therefore, it could not be easily ported to alternative implementation targets.

3) *Narrow Focus on Datapath Synthesis:* Many HLS tools focus primarily on datapath synthesis, while leaving other important aspects unattended, such as interfaces to other hardware/software modules and platform integration. Solving the system integration problem then becomes a critical design bottleneck, limiting the value in moving to a higher-level design abstraction for IP in a design.

4) *Lack of Satisfactory QoR:* When early HLS tools were introduced in the mid-1990s to early-2000s, the EDA industry was still struggling with timing closure between logic and physical designs. There was no dependable RTL to GDSII foundation to support HLS, which made it difficult to consistently measure, track, and enhance HLS results. Highly automated RTL to GDSII solutions only became available in late-2000s (e.g., provided by the IC Compiler from Synopsys [116] or the BlastFusion/Talus from Magma [113]). Moreover, many HLS tools were weak in optimizing real-life design metrics. For example, many commonly used algorithms in the synthesis engine focused on reducing functional unit count and latency, which do not necessarily correlate to actual silicon area, power, and performance. As a result, the final implementation often fails to meet timing/power requirements. Another major factor limiting QoR was the limited capability of HLS tools to exploit performance-optimized and power-efficient IP blocks on a specific platform, such as the versatile DSP blocks and on-chip memories on modern FPGA platforms. Without the ability to match the QoR achievable with an RTL design flow, most designers were unwilling to explore potential gains in design productivity.

5) *Lack of a Compelling Reason/Event to Adopt a New Design Methodology:* The first-generation HLS tools were clearly ahead of their time, as the design complexity was still manageable at the RTL in late-1990s. Even though the

second-generation of HLS tools showed interesting capabilities to raise the level of design abstraction, most designers were reluctant to take the risk of moving away from the familiar RTL design methodology to embrace a new unproven one, despite its potential large benefits. Like any major transition in the EDA industry, designers needed a compelling reason or event to push them over the "tipping point," i.e., to adopt the HLS design methodology.

Another important lesson learned is that tradeoffs must be made in the design of the tool. Although a designer might wish for a tool that takes any input program and generates the "best" hardware architecture, this goal is not generally practical for HLS to achieve. Whereas compilers for processors tend to focus on local optimizations with the sole goal of increasing performance, HLS tools must automatically balance performance and implementation cost using global optimizations. However, it is critical that these optimizations be carefully implemented using scalable and predictable algorithms, keeping tool runtimes acceptable for large programs and the results understandable by designers. Moreover, in the inevitable case that the automatic optimizations are insufficient, there must be a clear path for a designer to identify further optimization opportunities and execute them by rewriting the original source code.

Hence, it is important to focus on several design goals for a HLS tool.

a) *Capture designs at a bit-accurate, algorithmic level*. The source code should be readable by algorithm specialists.
b) *Effectively generate efficient parallel architectures with minimal modification* of the source code, for parallelizable algorithms.
c) *Allow an optimization-oriented design process*, where a designer can improve the QoR by successive code modification, refactoring and refinement on synthesis options/directives.
d) *Generate implementations that are competitive* with synthesizable RTL designs after automatic and manual optimization.

We believe that the tipping point for transitioning to HLS methodology is happening now, given the reasons discussed in Section I and the conclusions by others [14], [85]. Moreover, we are pleased to see that the latest generation of HLS tools has made significant progress in providing wide language coverage and robust compilation technology, platform-based modeling, and advanced core HLS algorithms. We shall discuss these advancements in more detail in the next few sections.

III. State-of-Art of HLS Flow for FPGAs

AutoPilot is one of the most recent HLS tools, and is representative of the capabilities of the state-of-art commercial HLS tools available today. Fig. 1 shows the AutoESL AutoPilot development flow targeting Xilinx FPGAs. AutoPilot accepts synthesizable ANSI C, C++, and OSCI SystemC (based on the synthesizable subset of the IEEE-1666 standard [115]) as input and performs advanced platform-based code transformations

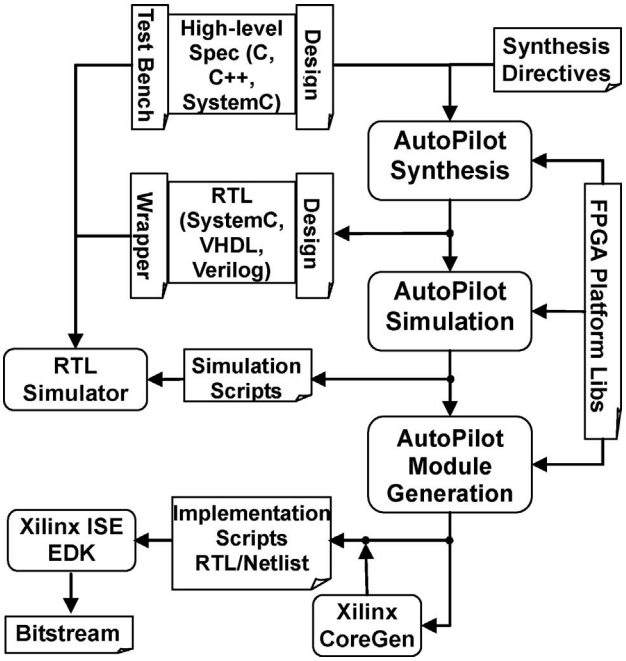

Fig. 1. AutoESL and Xilinx C-to-FPGA design flow.

and synthesis optimizations to generate optimized synthesizable RTL.

AutoPilot outputs RTL in Verilog, VHDL or cycle-accurate SystemC for simulation and verification. To enable automatic co-simulation, AutoPilot creates test bench (TB) wrappers and transactors in SystemC so that the designers can leverage the original test framework in C/C++/SystemC to verify the correctness of the RTL output. These SystemC wrappers connect high-level interfacing objects in the behavioral TB with pin-level signals in RTL. AutoPilot also generates appropriate simulation scripts for use with third-party RTL simulators. Thus, designers can easily use their existing simulation environment to verify the generated RTL.

In addition to generating RTL, AutoPilot also creates synthesis reports that estimate FPGA resource utilization, as well as the timing, latency, and throughput of the synthesized design. The reports include a breakdown of performance and area metrics by individual modules, functions, and loops in the source code. This allows users to quickly identify specific areas for QoR improvement and then adjust synthesis directives or refine the source design accordingly.

Finally, the generated HDL files and design constraints feed into the Xilinx RTL tools for implementation. The Xilinx integrated synthesis environment (ISE) tool chain (such as CoreGen, XST, and PAR) and Embedded Development Kit (EDK) are used to transform that RTL implementation into a complete FPGA implementation in the form of a bitstream for programming the target FPGA platform.

IV. Support of High-Level Programming Models

In this section, we show that it is important for HLS to provide wide language coverage and leverage state-of-the-art compiler technologies to achieve high-quality synthesis results.

TABLE I
USEFUL LANGUAGE FEATURES FOR EFFECTIVE C/C++-BASED DESIGN AND SYNTHESIS

Language	Constructs	Benefits
C	Arbitrary-precision integer types	Bit-accurate design QoR
	Floating-point types	Floating-point arithmetic
	Function calls	Modular design hierarchy
	Pointers	Efficiency and flexibility
	Structs and unions	Data encapsulation
C++	Fixed-point types	Fixed-point arithmetic Accuracy-cost tradeoff
	Templates	Parameterizable design
	Classes	Object-oriented modeling (encapsulation, inheritance, polymorphism, and others)
SystemC	Modules and processes	Coarse-grained concurrency
	Clocks	Custom protocol Multi-clock design
	TLM	Fast simulation

A. Robust Support of C/C++ Based Synthesis

Comprehensive language coverage is essential to enabling wide acceptance of C/C++ based design and synthesis. The reasons are twofold.

1) *Reduced verification effort*: A broad synthesizable subset minimizes the required code changes to convert the reference C source into a synthesizable specification. This effectively improves the design productivity and reduces or eliminates the additional verification effort to ensure equivalence between the synthesizable code and the original design.
2) *Improved design quality*: Comprehensive language support allows designers to take full advantage of rich C/C++ constructs to maximize simulation speed, design modularity, and reusability, as well as synthesis QoR.

However, it is quite challenging to compile an input specification in software C language, which is known for its highly flexible syntax and semantic ambiguities, into a well-structured and well-optimized hardware described in HDL.

In fact, many early C-based synthesis tools only handle a very limited language subset, which typically includes the native integer data types (e.g., *char*, *short*, and *int*), 1-D arrays, *if-then-else* conditionals, and *for* loops. Such language coverage is far from sufficient to allow complex large-scale designs. As shown in Table I, supporting more advanced language features in C, C++, and SystemC is critical to raising the level of design abstraction and enabling efficient HLS.

AutoPilot accepts three standard C-based design entries in ANSI C, C++, and SystemC. It provides robust synthesis technologies to efficiently handle different aspects of the C/C++ language, such as data type synthesis (for both primitive and composite types), pointer synthesis, memory synthesis, control synthesis, loop synthesis, modular hierarchy synthesis (for functions, classes, and concurrent modules), and interface synthesis (for parameters and global variables).

Designers can fully control the data precisions of a C/C++ specification. AutoPilot supports single and double-precision floating-point types and efficiently utilizes the floating-point IPs provided by the FPGA platforms. Common floating-point math routines (e.g., square root, exponentiation, and logarithm) can be mapped to highly optimized device-specific IPs.

In addition, AutoPilot has the capabilities to simulate and synthesize arbitrary-precision integers (*ap_int*) and fixed-point data types (*ap_fixed*). The arbitrary-precision fixed-point (*ap_fixed*) data types support all common algorithmic operations. With this library, designers can explore the accuracy and cost tradeoff by modifying the resolution and fixed-point location and experimenting with various quantization and saturation modes.

AutoPilot also supports the OCSI synthesizable subset [115] for SystemC synthesis. Designers can make use of SystemC bit-accurate data types (sc_int/sc_uint, sc_bigint/sc_biguint, and sc_fixed/sc_ufixed) to define the data precisions. They can also create parallel hierarchical designs with concurrent processes running inside multiple modules.

B. Use of State-of-the-Art Compiler Technologies

AutoPilot tightly integrates the LLVM compiler infrastructure [60], [112] to leverage leading-edge compiler technologies. LLVM features a GCC-based C/C++ front end called *llvm-gcc* and a newly developed source code front end for C/C++ and Object C/C++ called *Clang*, a virtual instruction set based on a type-safe static single-assignment (SSA) form [24], a rich set of code analyses and transformation passes, and various back ends for common target machines.

AutoPilot uses the *llvm-gcc* front end to obtain an intermediate representation (IR) based on the LLVM instruction set. On top of this IR, AutoPilot performs a variety of compiler transformations to aggressively optimize the input specification. The optimization focuses on reducing code complexity and redundancy, maximizing data locality, and exposing parallelism.

In particular, the following classes of transformations and analyses have shown to be very useful for hardware synthesis.

1) SSA-based code optimizations such as constant propagation, dead code elimination, and redundant code elimination based on global value numbering [2].
2) Expression rewriting such as strength reduction and arithmetic simplification to replace expensive operations and expressions with simpler ones [e.g., $x\%2^n = x\&(2^n-1)$, $3*x-x = x<<1$].
3) Range analysis and bitwidth analysis [21], [81] that extract and propagate the value range information throughout the program to reduce bitwidths of variables and operations.
4) Sophisticated alias analysis and memory dependence analysis [51] that analyzes data and control dependences to discover parallelism between pointer and array accesses.

5) Memory optimizations such as memory reuse, array scalarization, and array partitioning [19] to reduce the number of memory accesses and improve memory bandwidth.
6) Loop transformations such as unrolling, loop fusion, and loop rotation to expose loop-level parallelism [51].
7) Function optimizations such as inlining and pointer-to-scalar argument promotion to enable code optimization across the function boundaries.

It is worth noting that the LLVM-based IR is in a language-agnostic format. In other words, the code can be optimized without considering the source language. As a result, the same set of analyses and optimizations on this representation can be shared and taken advantage of by many different language front ends.

Furthermore, unlike other conventional C/C++ compilers, which are typically designed to optimize with the native data types (e.g., *char*, *short*, *int*, and *long*), LLVM and AutoPilot compilation and transformation procedures are fully bit accurate. This is a significant advantage for hardware synthesis since bit-level redundancy and parallelism can be well optimized and well exploited [94].

V. Platform-Based Approach

In this section, we discuss the platform-based synthesis methodology used by AutoPilot targeting Xilinx FPGAs.

A. Platform Modeling for Xilinx FPGAs

AutoPilot uses detailed target platform information to carry out informed and target-specific synthesis and optimization. The platform specification describes the availabilities and characteristics of important system building blocks, including the available computation resources, memory resources, and communication interfaces on a given Xilinx FPGA device.

Component pre-characterization is involved in the modeling process. Specifically, it characterizes the delay, area, and power for each type of hardware resource, such as arithmetic units (e.g., adders and multipliers), memories [e.g., random access memories (RAMs), read-only memories, and registers], steering logic (multiplexors), and interface logic (e.g., FIFOs and bus interface adapters). The delay/area/power characteristic curves are derived by varying the bit widths, number of input and output ports, pipeline intervals, and latencies. The resulting characterization data is then used to make implementation choices during synthesis.

Notably, the cost of implementing hardware on FPGAs is often different from that for ASIC technology. For instance, most designs include multiplexors to route data to different points in a design, share hardware resources, and initialize the state of the system. On FPGAs, multiplexors typically have the same cost and delay as an adder [approximately one lookup table (LUT)/output]. In some cases, however, a multiplexor can merge with other logic, such as a downstream adder or multiplexor, resulting in no additional hardware cost. In contrast, in ASIC technology, multiplexors are typically significantly less expensive than adders and other arithmetic operations and this cost cannot typically be eliminated by technology mapping. As a result, understanding the cost and delay of multiplexing operations is critical to building optimized FPGA designs.

FPGA technology also features heterogeneous on-chip resources, including not only LUTs and flip flops but also other prefabricated architecture blocks such as DSP48s and Block RAMs. Understanding the tradeoff between these heterogeneous resources is critical for efficient FPGA mapping. For instance, in FPGAs logic functions are significantly more expensive relative to memory than in ASIC technology, since logic functions must be implemented using LUTs and flip flops in the FPGA fabric whereas memory is usually implemented using Block RAMs which exist as customized SRAM cells in the FPGA. Furthermore, smaller memories and shift registers may be more efficiently mapped to LUT cells or flip flops in the FPGA than to Block RAM, adding additional complexity for memory characterization.

Such FPGA-specific platform information is carefully modeled for each and every FPGA device family, and considered by AutoPilot during synthesis for performance and area tradeoff. In addition, AutoPilot has the capability of detecting certain computation patterns and mapping a group of operations to platform-specific architecture blocks, such as DSP48 blocks, or predefined customer IPs.

B. Integration with Xilinx Toolset

In order to raise the level of design abstraction more completely, AutoPilot attempts to hide details of the downstream RTL flow from users as much as possible. Otherwise, a user may be overwhelmed by the details of vendor-specific tools such as the formats of constraint and configuration files, implementation and optimization options, or directory structure requirements.

As shown in Fig. 1, AutoPilot implements an end-to-end C-to-FPGA synthesis flow integrated with the Xilinx toolset in several areas.

1) *ISE integration*: AutoPilot automatically generates scripts and constraints for Xilinx ISE from the high-level constraints entered in AutoPilot. AutoPilot can also directly invoke ISE from within the tool to execute the entire C-to-FPGA flow and extract the exact resource utilization and the final timing from the ISE reports. For advanced users who are familiar with the Xilinx tool flow, AutoPilot also provides options to tune the default implementation and optimization settings, such as I/O buffer insertion, register duplication/balancing, and place-and-route effort.
2) *CoreGen integration*: AutoPilot can automatically generate optimized IP blocks, such as memories, FIFOs, and floating-point units, using Xilinx Core Generator (CoreGen). In some cases, the CoreGen implementations are superior to the comparable functions implemented through logic synthesis resulting in better QoR. The resulting CoreGen netlists are also incorporated and encapsulated without further user intervention.
3) *EDK integration*: The hardware modules synthesized by AutoPilot can also be integrated into the Xilinx EDK environment for system-level hardware/software

co-design and exploration. Specifically, AutoPilot is capable of generating various bus interfaces, such as Xilinx fast simplex link and processor local bus for integrating with MicroBlaze and PowerPC processors and Xilinx native port interface (NPI) for integrating with external memory controllers. AutoPilot instantiates these interfaces along with adapter logic and appropriate EDK meta-information to enable generated modules be quickly connected in an EDK system.

VI. Advances in Synthesis and Optimization Algorithms

In this section, we highlight some recent algorithmic advancement in HLS that we believe are important factors in improving the QoRs of the latest HLS tools and helping them to produce results that are competitive with manual designs.

A. Efficient Mathematical Programming Formulations to Scheduling

Classical approaches to the scheduling problem in HLS use either conventional heuristics such as list scheduling [1] and force-directed scheduling [74], which often lead to sub-optimal solutions, due to the nature of local optimization methods, or exact formulations such as integer-linear programming [46], which can be difficult to scale to large designs. Recently, an efficient and scalable system of difference constraint (SDC)-based linear-programming formulation for operation scheduling has been proposed [15]. Unlike previous approaches which use $O(m \times n)$ binary variables to encode a scheduling solution with n operations and m steps [46], SDC uses a continuous representation of time with only $O(n)$ variables; for each operation i, a scheduling variable s_i is introduced to represent the time step at which the operation is scheduled. By limiting each constraint to the integer-difference form, that is

$$s_i - s_j \leq d_{ij}$$

where d_{ij} is an integer, it is shown that a totally unimodular constraint matrix can be obtained. A totally unimodular matrix defined as a matrix whose every square submatrix has a determinant of 0 or ± 1. A linear program with a totally unimodular constraint matrix is guaranteed to have integral solutions. Thus, an optimal integer solution can be obtained without expensive branch-and-bound procedures.

Many commonly encountered constraints in HLS can be expressed in the form of integer-difference constraints. For example, data dependencies, control dependencies, relative timing in I/O protocols, clock frequencies, and latency upper-bounds can all be expressed precisely. Some other constraints, such as resource usage, cannot directly fit into the form. In such cases, approximations can be made to generate pair-wise orderings which can then be expressed as integer-difference constraints. Other complex constraints can be handled in similar ways, using approximations or other heuristics. Thus, this technique provides a very flexible and versatile framework for various scheduling problems, and enables highly efficient solutions with polynomial time complexity.

B. Soft Constraints and Applications for Platform-Based Optimization

In a typical synthesis tool, design intentions are often expressed as constraints. While some of these constraints are essential for the design to function correctly, many others are not. For example, if the estimated propagation delay of a combinational path consisting of two functional units is 10.5 ns during scheduling, while the required cycle time is 10 ns, a simple method would forbid the two operations to execute in one clock cycle. However, it is possible that a solution with a slight nominal timing violation can still meet the frequency requirement, considering inaccuracy in interconnect delay estimation and various timing optimization procedures in later design stages, such as logic refactoring, retiming, and interconnect optimization. In this case, strict constraints eliminate the possibility of improving other aspects of the design with some reasonable estimated violations. In addition, inconsistencies in the constraint system can occur when many design intentions are added—after all, the design is often a process of making tradeoffs between conflicting objectives.

A solution to the above problems is proposed in [20] using soft constraints in the formulation of scheduling. The approach is based on the SDC formulation discussed in the preceding section, but allows some constraints to be violated. Consider the scheduling problem with both hard constraints and soft constraints formulated as follows:

$$\begin{array}{lll} \text{minimize} & c^T s & \text{linear objective} \\ \text{subject to} & \boldsymbol{G}s \leq p & \text{hard constraints} \\ & \boldsymbol{H}s \leq q & \text{soft constraints.} \end{array}$$

Here, $\boldsymbol{G}$ and $\boldsymbol{H}$ correspond to the matrices representing hard constraints and soft constraints, respectively, and they are both totally unimodular as shown in [15]. Let $\boldsymbol{H}_j$ be the jth row of $\boldsymbol{H}$, for each soft constraint $\boldsymbol{H}_j s \leq q_j$, we introduce a violation variable v_j to denote the amount of violation and transform the soft constraint into two hard constraints as follows:

$$\begin{aligned} \boldsymbol{H}_j s - v_j &\leq q_j \\ -v_j &\leq 0. \end{aligned}$$

At the same time, we introduce a penalty term $\phi_j(v_j)$ to the objective function, to minimize the cost for violating the jth soft constraint. The final formulation becomes as follows:

$$\begin{array}{ll} \text{minimize} & c^T s + \Sigma_j \phi_j(v_j) \\ \text{subject to} & \boldsymbol{G}s \leq p \\ & \boldsymbol{H}s - v \leq q \\ & -v \leq 0. \end{array}$$

It can be shown that the new constraint matrix is also totally unimodular. If the amount of penalty is a convex function of the amount of violation, the problem can be solved optimally within polynomial time. Otherwise, convex approximations can be made in an iterative manner [20].

The overall flow of a scheduler using this method is shown in Fig. 2. Hard constraints and soft constraints are generated

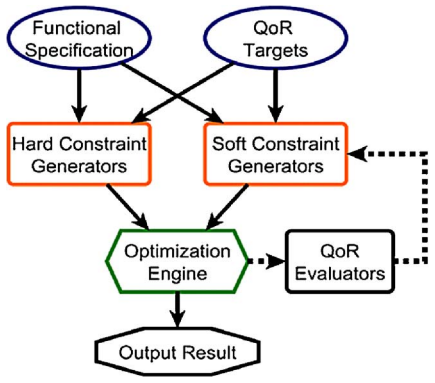

Fig. 2. Structure of a scheduler using both hard constraints and soft constraints.

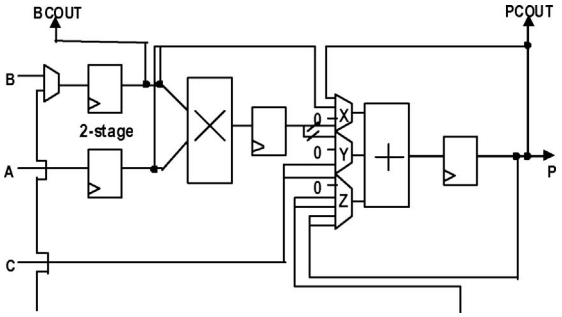

Fig. 3. Xilinx DSP48E block.

based on the functional specification and QoR targets. The constraints are fed to an optimization engine that uses a mathematical programming solver. The soft constraints can be updated, based on existing results and possibly new design intentions. The use of soft constraints provides a way to handle multiple conflicting design intentions simultaneously, leading to efficient global optimization using a mathematical programming framework. This approach offers a powerful yet flexible framework to address various considerations in scheduling.

To illustrate the use of soft constraints in HLS for FPGAs, we apply it to the problem of efficient utilization of built-in fabrics on FPGA platforms. Take the DSP48E block in Xilinx Virtex 5 FPGAs for example; each of the DSP48E blocks (sketched in Fig. 3) contains a multiplier and a post-adder, allowing efficient implementations of multiplication and multiply-accumulation. To fit the pattern of a DSP block, it is preferable that the operations are scheduled following certain relative cycle distances. Specifically, the addition should occur one cycle after the multiplication finishes to be mapped to the post-adder. In the constraint system, it is $s_+ - s_\times \leq l_\times$, where $l_\times$ is the number of stages the multiplication takes. These preferences can be nicely modeled by soft constraints as they are not required for a correct implementation but highly preferred to achieve good QoR on FPGAs.

C. Pattern Mining for Efficient Sharing

A typical target architecture for HLS may introduce multiplexors when functional units, storage units, or interconnects are shared by multiple operations/variables in a time-multiplexed manner. However, multiplexors (especially large ones) can be particularly expensive on FPGA platforms. Thus, careless decisions on resource sharing could introduce more overhead than benefit. In [16], a pattern-based approach for resource sharing is proposed. The method tries to extract common structures or patterns in the data-flow graph, so that different instances of the same pattern can share resources with little overhead. The approach tolerates small variations on port, bitwidth, operation types, and others, by using the graph editing distance as a metric to measure the similarity of two patterns. A systematic method for subgraph enumeration is developed which avoids generating redundant subgraphs. Pruning techniques are proposed based on characteristic vectors and locality-sensitive hashing. Instances of the same pattern are scheduled in the same way and conflicts are avoided when possible so that they can share resources, leading to resource reductions. This technique has been extended to pattern extraction and sharing in control data flow graphs [18].

D. Memory Analysis and Optimizations

While application-specific computation platforms such as FPGAs typically have considerable computational capability, their performance is often limited by available communication or memory bandwidth. Typical FPGAs, such as the Xilinx Virtex series, have a considerable number of block RAMs. Using these RAMs effectively is critical to meet performance target in many designs. This often requires partitioning elements of an array across multiple physical memory blocks to enable simultaneous access to different elements of the array.

In [19], a technique for automatic memory partitioning is proposed to increase throughput and reduce power for pipelined loops. It tightly integrates front-end transformations and operation scheduling in an iterative algorithm and has the ability to handle irregular array access, in addition to affine accesses. An example of memory partition is shown in Fig. 4. Consider a loop that accesses array A with subscripts i, $2\times i+1$, and $3\times i+1$, in the ith iteration. When the array is partitioned into two banks, the first contains elements with even indices and the second contains those with odd indices. If the loop is targeted to be pipelined with the initiation interval of one, i.e., a new loop iteration starts every clock cycle, the schedule in Fig. 4(b) will lead to port conflicts, because $(i + 1)$ mod $2 = (2 \times (i + 1) + 1)$ mod $2 = (3 \times i + 1)$ mod 2, when i is even; this will lead to three simultaneous accesses to the first bank. On the contrary, the schedule in Fig. 4(c) can guarantee at most two simultaneous accesses. Because $(i + 2)$ mod $2 \neq (3 \times i + 1)$ mod 2 for any i, *R1* and *R3* will never access the same bank in the same cycle. The method in [19] presents a theorem to capture all possible reference conflicts under cyclic partitioning in a data structure called a *conflict graph*. Then, an iterative algorithm is used to perform both scheduling and memory partitioning guided by the conflict graph.

VII. Advances in Simulation and Verification

Besides the many advantages of automated synthesis, such as quick design space exploration and automatic complex

```
for (i = 0; i < N; i++) {
    A[i] = …;           // R1
    A[2 * i + 1] = …;   // R2
    A[3 * i + 1] = …;   // R3
}
```

(a)

	Step 1	Step 2	Step 3
Iteration 1	A[i] A[2*i+1]	A[3*i+1]	
Iteration 2		A[i+1] A[2*(i+1)+1]	A[3*(i+1)+1]
Iteration 3			A[i+2] A[2*(i+2)+1]

(b)

	Step 1	Step 2	Step 3
Iteration 1	A[i] A[2*i+1]		A[3*i+1]
Iteration 2		A[i+1] A[2*(i+1)+1]	
Iteration 3			A[i+2] A[2*(i+2)+1]

(c)

Fig. 4. Example of memory partitioning and scheduling for throughput optimization. (a) Loop to be pipelined. (b) First schedule with partition. (c) Second schedule with partition.

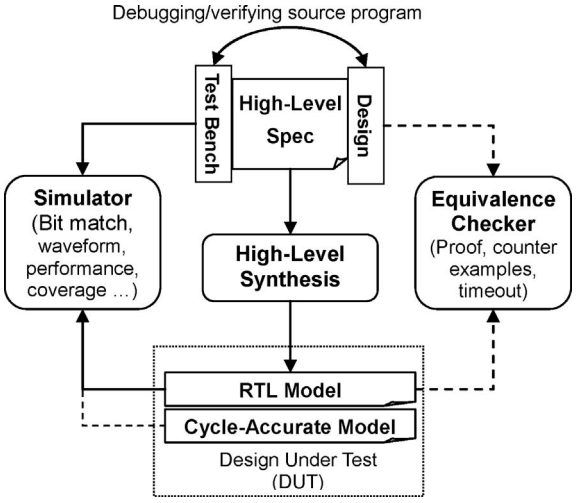

Fig. 5. HLS simulation and verification framework.

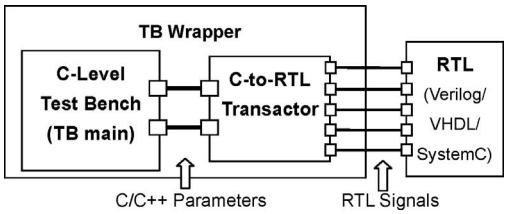

Fig. 6. Automatic RTL TB generation and connection in AutoPilot.

architectural changes like pipelining, resource sharing, and scheduling, HLS also enables a more efficient debugging and verification flow at the higher abstraction levels. Since HLS provides an automatic path to implementable RTL from behavioral/functional models, designers do not have to wait until manual RTL models become available to conduct verification. Instead, they can develop, debug and functionally verify a design at an earlier stage with high-level programming languages and tools. This can significantly reduce the verification effort due to the following reasons.

1) It is easier to trace, identify, and fix bugs at higher abstraction levels with more compact and readable design descriptions.
2) Simulation at the higher level is typically orders of magnitude faster than RTL simulation, allowing more comprehensive tests and greater coverage.

Fig. 5 captures a typical simulation and verification framework offered by state-of-the-art C-based HLS tools. In this flow designers usually start from high-level specification in C/C++ or SystemC. They use software programming and debugging tools, such as GCC/GDB, Valgrind, or Visual Studio, to ensure that the design is sufficiently tested and verified against a properly constructed TB. Once the input description to HLS is clean, designers can focus on the synthesis aspects and generate one or multiple versions of RTL code to explore the QoR tradeoffs under different performance, area, and power constraints. To confirm the correctness of the final RTL, designers can use the automatic co-simulation and/or formal equivalence checking provided by this framework.

A. Automatic Co-Simulation

At present, simulation is still the prevalent technique to check if the resulting RTL complies with the high-level specification. To reduce effort spent on RTL simulation, the latest HLS technologies have made important improvements on automatic co-simulation [3], [8], [87], allowing direct reuse of the original test framework in C/C++ to verify the correctness of the synthesized RTL.

As an example, Fig. 6 shows a block diagram describing how AutoPilot bridges a behavioral TB and RTL with an automatically constructed transactor and wrapper in SystemC. A C-to-RTL transactor is created to connect high-level interfacing constructs (such as parameters and global variables) with pin-level signals in RTL. This step involves data type synthesis as well as interface synthesis since the transactor needs to correctly translate various C/C++ data types and handle different interface protocols such as handshaking, streaming, and memory mapped I/O. Additionally, a SystemC wrapper is generated that combines the C-level TB and transactor. This wrapper also includes additional control logic to manage the communication between the testing module and the RTL design under test (DUT). For instance, a pipelined design may require that the TB feed input data into the DUT at a fixed rate.

This style of automatic co-simulation also helps designers avoid the timing-consuming manual creation of an RTL TB. Along with the use of instrumentation and code coverage tools, this flow can provide additional performance and code coverage analyses on the RTL output. Many HLS tools also generate

alternative cycle-accurate models (typically in SystemC) of the synthesized design that can be more quickly simulated than HDL.

B. Equivalence Checking

While formal equivalence checking tools for RTL-to-RTL and RTL-to-gate comparisons have been in production use for years, high-level to RTL checking is still an evolving technology.

Nevertheless, promising progress on C-to-RTL equivalence checking has been made in recent years, especially from industry. For instance, the Sequential Logic Equivalence Checker from Calypto [106] can identify mismatches between a synthesizable C/C++/SystemC model and an RTL design without the need of a TB. This tool has been integrated in several commercial HLS flows. Synopsys has also presented their Hector tool in [54], which integrates multiple bit-level and word-level equivalence checking techniques, such as automatic test pattern generation, binary decision diagram, Boolean satisfiability, and satisfiability modulo theories to address the system level to RTL formal verification problem.

An excellent survey of the sequential equivalence checking (SEC) techniques is given in [64], with discussions of their usage in real-world HLS flows. As mentioned in this paper, the current SEC technology can handle moderate design size with gate count between 500K and 700K gates and tolerate latency differences between high-level and RTL models on the order of hundreds of clock cycles. Beyond this range, further design partitioning is required to help the checker to reduce the verification complexity.

Currently, formal equivalence checking plays a supporting role in the verification flow for HLS. This is particularly true for FPGA designs, where in-system simulation is possible with much wider simulation coverage. Design iterations can be performed quickly and inexpensively without huge manufacturing cost. However, multiple challenges remain to be addressed with in-system debugging using HLS methodology, about which we shall further elaborate in Section X.

VIII. Integration with Domain-Specific Design Platforms

The time-to-market of an FPGA system design is dependent on many factors, such as availability of reference designs, development boards, and in the end, FPGA devices themselves. Primarily, HLS only addresses one of these factors: the ability of a designer to capture new algorithms and implement an RTL architecture from the algorithm. Reducing the overall time-to-market requires not only reducing the design time, but also integrating the resulting design into a working system. This integration often includes a wide variety of system-level design concerns, including embedded software, system integration, and verification [105]. Hence, it is crucial that such integration can be performed as easily and as quickly as possible.

A view of an integrated design is shown in Fig. 7. The interface cores (marked GigE, PCI, DVI, and LVDS in the figure) are implemented in low-level RTL code and are provided as encapsulated IP cores. These cores tend to have

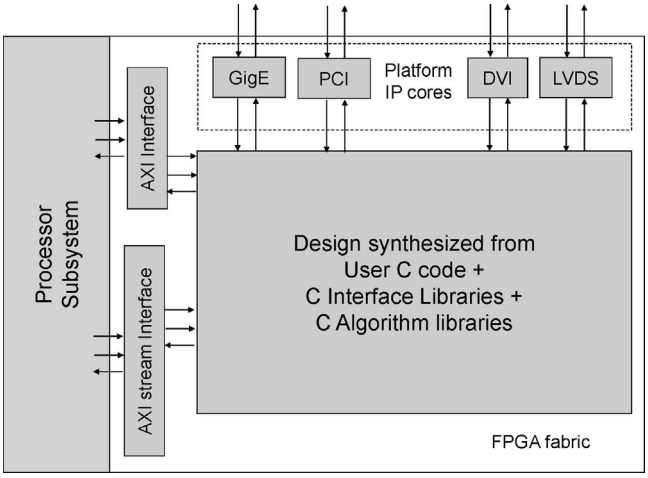

Fig. 7. Block diagram showing an algorithmic block integrated with a processor and I/O.

tight requirements on circuit architecture in order to function correctly, and often have specific timing constraints, placement requirements, and instantiated architectural primitives. As a result, these cores are not easily amenable to HLS and form part of the system infrastructure of a design. Note, however, that these cores represent a small portion of the overall design synthesized in the FPGA, where system designers are not likely to have significant differentiating ability.

A second key part of system infrastructure is the processor subsystem shown on the left of Fig. 7. Subsystem PSS is responsible for executing the relatively low-performance processing in the system.

The portion of a design generated using HLS represents the bulk of the FPGA design and communicates with the system infrastructure through standardized wire-level interfaces, such as AXI4 memory-mapped and streaming interfaces [97] shown in Fig. 7. These interfaces are abstracted in the C code to appropriate application-level interfaces, which can be simulated at a functional level in C code. In order to understand this abstract architecture model, we show some concrete examples of domain-specific design platforms that we used to build FPGA systems, one for video applications and another for cognitive radio designs.

A. Video Starter Kit

Video processing systems implemented in the FPGA include a wide variety of applications from embedded computer-vision and picture quality improvement to image and video compression. These systems also target a variety of end-markets ranging from television studio equipment to industrial imaging and consumer equipment, such as high-definition televisions (HDTVs) and digital cameras. Typically, these systems include two significant pieces of complexity. First, they must communicate by standardized interfaces, such as high-definition serial digital interface, high-definition multimedia interface (HDMI), or V-by-one, with other equipment in order to be demonstrated. Second, they often perform inter-frame processing, which almost always requires a large frame-buffer implemented in cheap external memory, such as DDR2 synchronous dynamic random access memory (SDRAM).

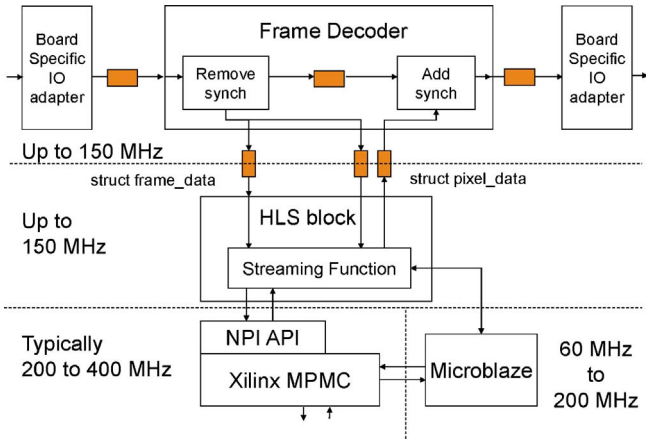

Fig. 8. Video processing architecture template.

To address these complexities and make it relatively straightforward for designers to implement video processing applications and demonstrate them in real-time on development boards, we have leveraged a portable platform methodology. This platform is derived from the Xilinx EDK-based reference designs provided with the Xilinx Spartan 3ADSP Video Starter Kit and has been ported to several Xilinx Virtex 5 and Spartan 6 based development boards, targeting high-definition video processing with pixel clocks up to 150 MHz. A block diagram is shown in Fig. 8.

Incoming video data is received using board and protocol specific interface adapters and formatted as a non-handshaked stream of RGB video data, with horizontal and vertical synchronization and data enable signals. When a board uses an external decoder chip which formats digital video in this way, such as the Spartan 3ADSP video Starter Kit, the I/O adapter can often be very simple, requiring almost no FPGA logic. In other cases, such as on the Xilinx University Program Atlys board [119] which implements HDMI interfaces entirely in FPGA logic, the interface logic can be more significantly complex.

The incoming video data is analyzed by the frame decoder block to determine the frame size of the incoming video, which is passed to the HLS block, enabling different video formats to be processed. The frame size, represented by *struct frame_data*, is sent to the HLS block first, followed by the given number of active video pixels without synchronization signals, represented by *struct pixel_data*. The synchronization signals themselves are encoded and delayed, before being reassembled with the processed video data and sent to the output video interface. This delay accommodates non-causal spatial filters with up to a small number of lines of delay, without requiring the output video to be shifted. Longer processing delays can be accommodated internally to the HLS block by a frame buffer by outputting the previously processed frame.

The application is typically partitioned between the HLS block and the Microblaze control processor. In video systems, the control processor often handles processing that occurs at the frame rate [typically 60 or 120 frames per second (f/s) for the majority of consumer video equipment], and can receive data analyzed from the incoming video, and generate parameter updates to the processing core. Simple processing tasks can be computed in the vertical blanking interval, while more complex tasks may require the entire frame time to compute, meaning that analysis of frame n is computed during the arrival of frame $n + 1$ and the results are used to update frame $n + 2$.

The HLS block itself is capable of processing video pixels at the full rate of the incoming video data, typically as a streaming dataflow pipeline generated from multiple loops in C code. To meet the pixel-rate requirements of HDTV systems, the HLS block typically process one new pixel per clock cycle in consumer grade FPGAs, such as the Xilinx Spartan 6 family. Video line buffers are synthesized directly from embedded FPGA memories, expressed as arrays in C code.

The interface to external memory used for frame buffers is implemented using the Xilinx multi-ported memory controller (MPMC) [120], which provides access to external memory to the HLS block and to the Microblaze control processor, if necessary. The MPMC provides a consistent user-level interface through the NPI [120] to a variety of memory technologies, abstracting the FPGA-architecture specific details of interfacing with correct timing to a particular external memory technology. NPI requires applications to explicitly specify large bursts in order to maximize memory bandwidth to burst-oriented memory technologies, such as DDR2 SDRAM. The RTL code generated by AutoPilot can leverage these bursts to directly implement video frame buffers and other patterns of memory accesses without a separate direct memory access (DMA) engine.

B. High-Level Design of Cognitive Radios Project

Cognitive radio systems typically contain both computationally intensive processing with high data rates in the radio processing, along with complex, but relatively low-rate processing to control the radio processing. Such systems can be elegantly described and quickly simulated in algorithmic C code, enabling opportunities to improve the system-level management algorithms. However, efficiently building such systems in FPGAs can be complex, since they involve close interaction between the processing code that must be implemented in the FPGA fabric to provide adequate performance, and the control code that would typically be implemented in an embedded processor. Although HLS provides a path to implementing the radio processing efficiently in FPGA logic, efficient interaction with the processor is an important part of the overall system complexity.

The target template architecture, shown in Fig. 9, is divided in two subsystems: a processor subsystem and an accelerator subsystem. The processor subsystem contains standard hardware modules and is capable of running a standard embedded operating system, such as Linux. These modules include the embedded central processing unit (CPU) (e.g., PowerPC or MicroBlaze), memory controller to interface to external DRAM, and I/O modules (e.g., Ethernet). The processor subsystem is responsible for two main tasks: executing the software runtime system in charge of the application control at runtime, and executing computationally non-intensive

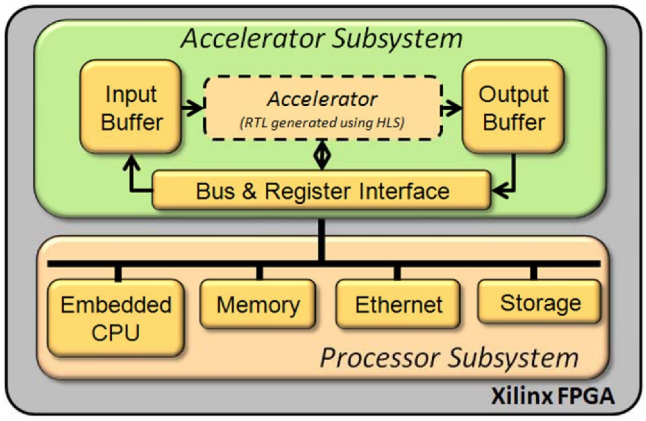

Fig. 9. Radio processing architecture template.

components in the application. The accelerator subsystem is used for implementing components with high computational requirements in hardware. In order to transfer data into and out of the accelerator subsystem, the *accelerator* block is connected to on-chip memories (i.e., standard interfaces). These on-chip memories are used as a shared-memory communication scheme between hardware and software components. The bus interface logic implements a DMA functionality to efficiently move data. A set of interface registers, accessible from software, is used for controlling hardware execution and accessing component parameters. The accelerator block is synthesized using the HLS tools.

To program the architecture, the application is captured as a pipeline of concurrent components or actors. Each actor conceptually executes either in the processor subsystem, or in the accelerator subsystem. Actors executing in the accelerator system also include a small proxy component executing in the processor, which is responsible for data transfer and synchronization with the FPGA hardware generated through HLS. This allows the component implementation to be completely abstracted, and a designer can implement individual components without knowing about the implementation details of other components or how they are logically interconnected. The composition of actors and the dataflow between them is described in an XML file, enabling new compositions to be easily described. Components also expose a configuration interface with multiple parameters, allowing them to be reconfigured in an executing system by user-defined control code executing in the processor subsystem.

IX. Design Experience and Results

In this section we summarize some recent design experiences using HLS for FPGA designs in the two application domains discussed in the preceding section and discuss the experimental results, especially in terms of the QoRs of HLS as compared to manual designs.

A. Summary of BDTI HLS Certification

Xilinx has worked with Berkeley Design Technology (BDTI), Inc. [100] to implement an HLS Tool Certification Program [101]. This program was designed to compare the results of an HLS Tool and the Xilinx Spartan 3 FPGA that is part of the Video Starter Kit, with the result of a conventional DSP processor and with the results of a good manual RTL implementation. There were two applications used in this Certification Program, an optical flow algorithm, which is characteristic for a demanding image processing application and a wireless application (DQPSK) for which a very representative implementation in RTL was available. The results of the certification of the AutoPilot tool from AutoESL are available on the BDTI website [102].

TABLE II
QoRs for BDTI Optical Flow Workflow Operating Point 2: Maximum Throughput, 1280 × 720 Progressive Scan

Platform	Chip Unit Cost (Qty 10K)	Maximum f/s	Cost Per f/s (Lower Is Better)
AutoESL AutoPilot plus Xilinx RTL tools targeting the Xilinx XC3D3400A FPGA	$26.65	183	$0.14
Texas Instruments software development tools targeting TMS320DM6437 DSP processor	$21.25	5.1	$4.20

Table reproduced from [102].

TABLE III
QoRs for DQPSK Receiver Workload: 18.75 MSamples/Second Input Data at 75 MHz Clock Speed (Table Reproduced from [102])

Platform	Chip Resource Utilization (Lower Is Better)
AutoESL AutoPilot plus Xilinx RTL tools targeting the Xilinx XC3D3400A FPGA	5.6%
Hand-written RTL code using Xilinx RTL tools targeting the Xilinx XC3SD3400A FPGA	5.9%

Results showing the maximum performance for the optical flow algorithm are included in Table II, comparing comparably priced consumer-grade FPGA and DSP targets. The AutoPilot implementation achieved approximately 30 times better throughput per dollar than the optimized DSP implementation. In addition, BDTI qualitatively assessed the "extent of modifications to the source code" necessary to implement the optical flow algorithm. The DSP processor implementation rated "fair," while the AutoPilot implementation rated "good," indicating that less source code modification was necessary to achieve high performance when using AutoPilot.

Results for the DQPSK application are shown in Table III, comparing the QoRs of the AutoPilot implementation with a manual RTL implementation. After optimization, including both significant source code refactoring and careful use of tool directives, the AutoPilot implementation achieved slightly lower resource usage than the RTL implementation. It is worth noting that the hand-written RTL made use of optimized Xilinx CoreGen IP blocks where applicable.

BDTI also assessed overall ease of use of the DSP tool flow and the FPGA tool flow, combining HLS with the low-level implementation tools. They concluded that the DSP tool flow was still significantly easier to use, primarily due to difficulties

installing the FPGA tools and a lack of sufficient platform infrastructure that can be accessed without in-depth knowledge of the FPGA tool flow. In the future, we believe that these issues will be solved as shown in Section VIII.

B. Sphere Decoder

Xilinx has implemented a sphere decoder for a multi-input multi-output wireless communication system using AutoPilot [68], [86]. The algorithm [29] consists largely of moderate-throughput linear algebra operations, such as matrix-matrix multiply, matrix inverse, QR decomposition, and vector-norm computations implemented on small-dimension matrices. The application exhibits a large amount of parallelism, since the operations must be executed on each of 360 independent subcarriers which form the overall communication channel and the processing for each channel can generally be pipelined. However, in order to reach an efficient high-utilization design, the implementation makes extensive use of resource sharing and time-division multiplexing, with the goal of simultaneously reducing resource usage and end-to-end processing latency.

The algorithm was originally implemented in MATLAB, which was converted to an algorithmic C model totaling approximately 4000 lines of code. The C model was further modified to generate an efficient implementation with AutoPilot. This code was converted to run through AutoPilot in a matter of days and optimized over a period of approximately three man-months. The resulting HLS code for the application makes heavy use of C++ templates to describe arbitrary-precision integer data types and parameterized code blocks used to process different matrix sizes at different points in the application. Various AutoPilot-specific *#pragma* directives were used, primarily to express the layout of arrays in memory blocks, to direct the unrolling and scheduling of loops to the appropriate level of parallelism, and to guide the scheduling algorithms to share operators and minimize resource usage. Most of the code included no explicit specification of the RTL structure, although in one case it was necessary to include a *#pragma* directive to force the RTL micro-architecture of a C function and to force the selection of a particular multiplier library element.

The end architecture consists of 25 independent actors in a streaming dataflow architecture, shown in Fig. 10. Each actor is separated by synthesized streams or double buffers from neighboring components, enabling them to execute concurrently. The portions marked "4 × 4," "3 × 3," and "2 × 2" perform the same algorithm on matrices of decreasing size, and are collectively termed the "channel preprocessor." These portions are implementing using parameterized C++ templates, targeted by AutoPilot at different II[1] (three in the 4 × 4 case, five in the 3 × 3 case, and nine in the 2 × 2 case), enabling optimized resource sharing decisions to be made automatically. The remainder of the design operates at $II = 1$, with all resource sharing described in the C code.

Table IV below summarizes the results, comparing the overall AutoPilot-based implementation with a previously reported RTL-style implementation built using Xilinx System Generator. Both designs were implemented as standalone cores using ISE 12.1, targeting Xilinx Virtex 5 speed grade 2 at 225 MHz. Using AutoPilot Version 2010.07.ft, we were able to generate a design that was smaller than the reference implementation in less time than a hand RTL implementation by refactoring and optimizing the algorithmic C model.

[1]II denotes initiation interval of the pipeline. $II = 1$ means the design accepts new inputs and produces new outputs at every clock cycle.

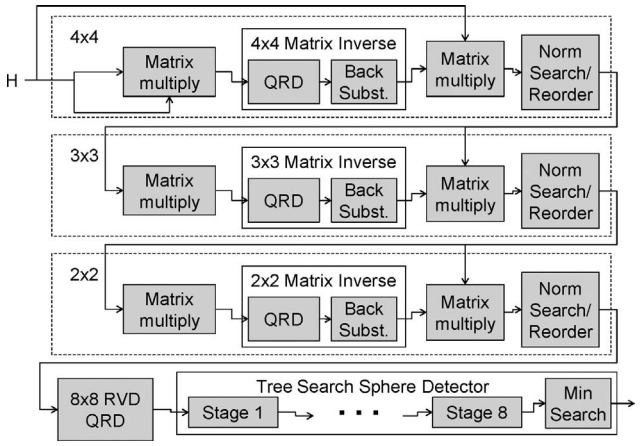

Fig. 10. Architecture of the sphere decoder application.

TABLE IV
SPHERE DECODER IMPLEMENTATION RESULTS

Metric	RTL Expert	AutoPilot Expert	Difference (%)
Dev. time (man-weeks)	16.5	15	−9
LUTs	32 708	29 060	−11
Registers	44 885	31 000	−31
DSP48s	225	201	−11
18K BRAMs	128	99	−26

Design time for the RTL design was estimated from work logs by the original authors of [29], and includes only the time for an algorithm expert and experienced tool user to enter and verify the RTL architecture in System Generator. Design time for the AutoPilot design was extracted from source code control logs. It reflects the time taken by a tool expert who is not a domain expert to take a piece of unfamiliar code, implement a first version in the tool, refactor the code to reflect a desired target architecture, reverse engineer the original RTL code to discover that algorithmic improvements were made in the RTL implementation that were not reflected back in the algorithmic model, and perform design exploration. In both cases, multiple people worked on the design in parallel. Given the significant time familiarizing ourselves with the application and structure of the code, we believe that an application expert familiar with the code would be able to create such a design at least twice as fast.

To better understand the area savings, it is instructive to look more closely at smaller blocks of the design. The real-valued QR decomposition (RVD-QRD) block, summarized in Table V, operates at $II = 1$, completing an 8 × 8 QR decomposition of 18-bit fixed point values every 64 cycles. The block implements a standard Givens-rotation based systolic

TABLE V
8 × 8 RVD-QRD IMPLEMENTATION RESULTS

Metric	RTL Expert	AutoPilot Expert	AutoPilot Expert
Dev. time (man-weeks)	4.5	3	5
LUTs	5082	6344	3862
Registers	5699	5692	4931
DSP48s	30	46	30
18K BRAMs	19	19	19

TABLE VI
MATRIX-MULTIPLY INVERSE IMPLEMENTATION RESULTS

Metric	4 × 4 RTL	4 × 4 AP	3 × 3 RTL	3 × 3 AP	2 × 2 RTL	2 × 2 AP
Dev. Time (man-weeks)	4	4	1	0	1	0
LUTs	9016	7997	6969	5028	5108	3858
Registers	11 028	7516	8092	4229	5609	3441
DSP48s	57	48	44	32	31	24
18K BRAMs	16	22	14	18	12	14

array consisting of diagonal and off-diagonal cells, where the diagonal cells compute an appropriate rotation, zeroing one of the matrix elements, and the off-diagonal cells apply this rotation to the other matrix elements in the same row. To meet the required throughput, one row of the systolic array is instantiated, consisting of one diagonal cell and eight off-diagonal cells, and the remaining rows are time multiplexed over the single row. In addition, since the systolic array includes a recurrence, 15 channels are time-division multiplexed over the same hardware.

Exactly the same architecture was implemented, although AutoPilot was able to generate a more optimized pipeline for the non-critical off-diagonal cell, resulting in slightly lower resource usage after optimization. After only three weeks, the AutoPilot design had met timing and throughput goals, but required more logic resources than the RTL design. After additional optimization and synthesis constraints on the DSP48 mapping, AutoPilot realized the same DSP48 mapping as the RTL design (three DSP48s to implement the off-diagonal cell rotations and six DSP48s to implement the diagonal cell computation and rotation), including mapping onto the DSP48 post-adder.

Table VI details multiple implementations of the "Matrix-Multiply Inverse" components, consisting of the combined Matrix Multiply, QR Decomposition, and Back Substitution blocks. This combination implements $(A^{\mathrm{T}}A)^{-1}$ for various dimensions of 18-bit complex fixed-point matrices. In both RTL and AutoPilot design approaches, the 4×4 case was implemented first, and the 3×3 and 2×2 cases were derived from the 4×4 case. In RTL, resource sharing was implemented in a similar way for each case, with real and imaginary components time-multiplexed over a single datapath. Deriving and verifying the 3×3 and 2×2 case took approximately one week each. In AutoPilot, the three cases were implemented as C++ template functions, parameterized by the size of the matrix. All three cases were implemented concurrently, using a script to run multiple tool invocations in parallel. Depending on the matrix dimension, different initiation intervals were targeted, resulting in a variety of resource sharing architectures for each block, as shown in Fig. 11.

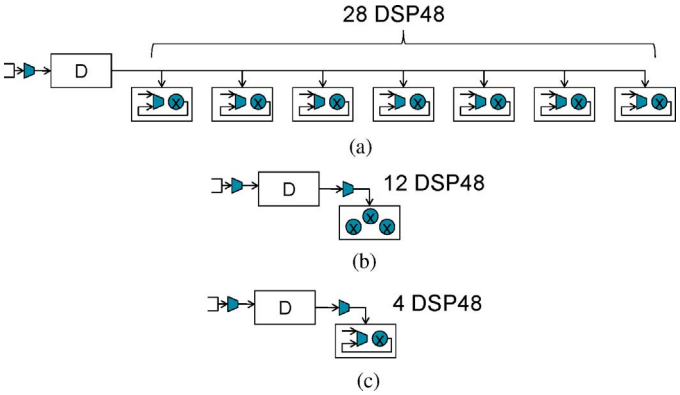

Fig. 11. Complex QRD architectures

In the 4×4 case, the off-diagonal cell implements fine-grained resource sharing, with one resource-shared complex multiplier. In the 3×3 case, the off-diagonal cell contains three complex multipliers and the off-diagonal cell itself is resource shared at a coarser granularity. In the 2×2 case, all of the off-diagonal cell operations are time multiplexed on a single complex multiplier, combining both coarse-grained and fine-grained resource sharing techniques. In AutoPilot, the only difference between these blocks is the different target initiation intervals, resulting in significant resource sharing. Certainly, there is no doubt that an RTL designer could have achieved these architectures, given the appropriate insight. However, getting to the optimized cases from the implemented 4×4 case would require a complete RTL-level redesign. We do observe that AutoPilot uses additional BRAM to implement this block relative to the RTL implementation, because AutoPilot requires tool-implemented double-buffers to only be read or written in a single loop. When considered as part of the overall design, however, we were able to reduce BRAM usage by converting BRAMs to LUTRAM due to the improve architecture of this block.

X. CONCLUSION AND CHALLENGES AHEAD

It seems clear that the latest generation of FPGA HLS tools has made significant progress in providing wide language coverage, robust compilation technology, platform-based modeling, and domain-specific system-level integration. As a result, they can quickly provide highly competitive QoRs, in many cases comparable or better than manual RTL designs. For the FPGA design community, it appears that HLS technology may be transitioning from research and investigation to selected deployment.

Despite this encouraging development, we also see many opportunities for HLS tools to further improve. In this section, we discuss a few directions and opportunities.

A. Support of Memory Hierarchy

The intelligent synthesis support of external off-chip memories is very important in applications that process large amounts of data or high data rates as follows.

1) Data-intensive video and image processing applications often require multiple frames of data to be stored. In practice, this storage is usually implemented using DDR2 SDRAMs and requires fast and efficient DMA logic to achieve high performance.
2) Recent advances in FPGA-based high-performance reconfigurable computing [33] also require efficient access to the gigabytes of external memories shared between a host processor and an FPGA accelerator.

However, as mentioned in [67], most of the existing HLS solutions currently lack efficient support of the memory hierarchy and sufficient abstraction of the external memory accesses. As a result, software designers are exposed to the low-level details of bus interfaces and memory controllers. They must be intimately familiar with the bus bandwidth and burst length and translate such knowledge to C code with substantial modifications. Clearly, such design practice is out of the comfort zone for many software developers and algorithm designers.

Hence, it is highly preferable to have synthesis tools hide explicit external memory transfers as much as possible from programmers. This would require the support of efficient memory hierarchies, including automatic caching and prefetching to hide memory latency and enhance data locality.

The CHiMPS project [77] is one of the promising attempts in this area. It incorporates a traditional memory hierarchy with caches into the synthesized FPGA system to manage external memory, while focusing on the highest possible performance from a given code without rewriting. The proposed C-to-FPGA compilation flow generates multiple distributed caches used by concurrent processing elements.

B. Higher-Level Models and Heterogeneous Computing

C and C++ languages are intended to describe sequential programs while modern FPGAs can implement highly complex concurrent systems. While the latest HLS tools have impressive capabilities to extract instruction-level and loop-level parallelism from C/C++ programs, it remains difficult to extract task-level parallelism from arbitrary sequential specifications. In addition, for systems with task-level feedback, sequential execution may not easily capture the parallel behavior of the system, making verification difficult.

Existing approaches mainly rely on manual annotation in the input specification for task-level parallelism. They also try to extract task-level parallelism by constructing synchronous data flow [61], Kahn process networks [49], or communicating sequential processes [45] models from a sequential specification. A more effective approach may be to use programming models that can explicitly specify concurrency, dependency, and locality. For instance, recent work used the CUDA language [108] for input specification to HLS [69] since CUDA can easily describe thread-level concurrency. However, CUDA was originally intended to model applications mapped onto NVIDIA graphics processing units (GPUs) and includes many GPU specific features which are not suitable for FPGAs. Our preference is to choose a device-neutral programming model. Currently, we are investigating the possibility of using Concurrent Collections [110] to describe the task level dependency while continuing to specify each task using C/C++ languages. We expect that such a high-level concurrent model is very useful for energy-efficient computing on customizable heterogeneous platforms, which include multi-core CPUs, GPUs, and FPGAs. This direction is being actively pursued in the newly established research center on customizable domain-specific computing [22], [107].

C. In-System Design Validation and Debugging

On-chip and on-board design validation and debugging has emerged as one of the most time-consuming aspects for FPGA-based systems, especially given continuously increasing device capacity and growing design complexity. Although the promise of HLS is that most verification can be performed by executing the original untimed C model, timing and data-related errors that occur on the board are often difficult to debug. At present, the common practice to detect such errors is to perform RTL-level timing accurate simulation or to use in-system debugging tools from major vendors (e.g., Altera SignalTap II and Xilinx ChipScope). These tools can be used to insert logic analyzer cores and provide capabilities to trigger and probe internal signals inside the FPGA circuits.

Debugging HLS designs at the RTL level is complicated by the fact that the structure of the original C code may not resemble the RTL architecture generated by an HLS tool. Many of the modern HLS solutions provide cross referencing capabilities between C and RTL to help designers understand the synthesis results. However, names in HDL are often transformed during RTL synthesis and technology mapping.

In order to effectively debug these systems, future HLS tools shall enable almost all debugging to occur in the C domain by providing the following.

1) *Debugging core synthesis*: the ability to synthesize efficient debugging logic with minimal overhead.
2) *Performance monitor generation*: the ability to watch the status of critical buffers to debug performance bugs, such as FIFO overflows and deadlocks.
3) *Step-through tracing*: the ability to set breakpoints at the C level and observe internal states from hardware blocks.

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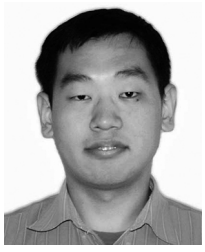

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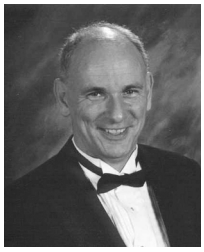

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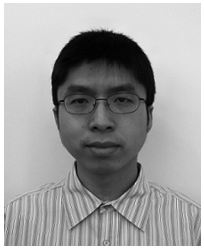

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