Networks on Chip : a very quick introduction!

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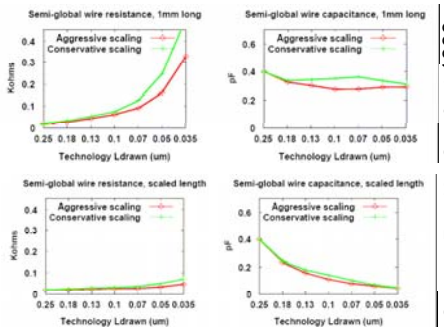
Overview of Talk

- Introduction
  - SoC Design Trends (communication centric design)
- Communication Centric Design
  - Application Modeling
  - Energy Modeling
  - NoC Optimization
- Conclusions

SoC Design Trends



Source: Ron Ho, Stanford 1999

Table 1: Power consumption of SoC components @ 200 Mhz

System Component	Part Name	Power (mW)
Embedded Processor	ARM946E-S[1]	60
Memory Controller	DW_ahb_memctl[2]	29.1
On-Chip Bus	DW_amba[2]	22.6
Cache	ARM946E-S[1]	36
Interrupt Controller	DW_ahb_ictl[2]	2.6
UART	DW_apb_uart[2]	4.1

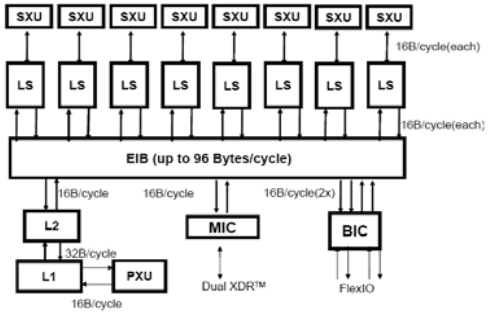
[1] http://www.arm.com/products/CPUs/ARM946ES.html
[2] Gate-level measurements of Synopsys Designware Library Cores

Source: Kanishka Lahiri 2004

- Focus on communication-centric design
  - Poor wire scaling
  - High Performance
  - Energy efficiency
    - Communication architecture large proportion of energy budget

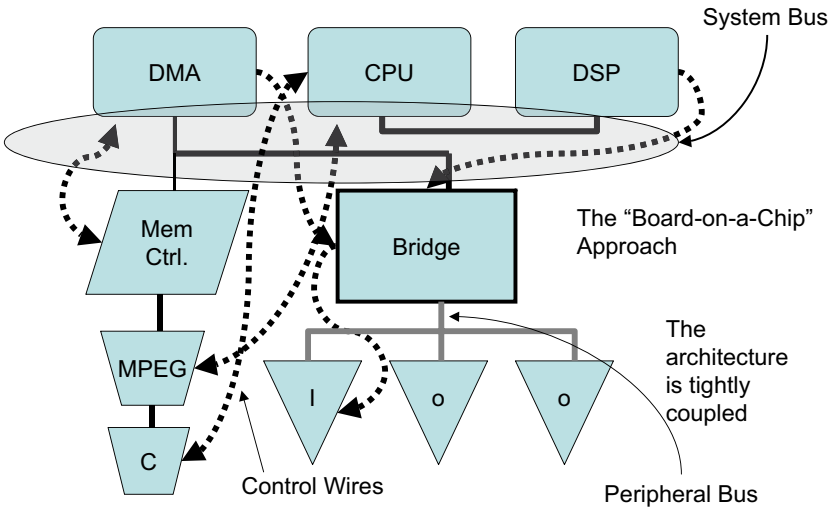
SoC Design Trends

- MPSoC: STI Cell
  - Eight Synergistic Processing Elements
  - Ring-based Element Interconnect Bus
    - 128-bit, 4 concentric rings
- Interconnect delays becoming important
  - Pentium 4 has two dedicated drive stages to transport signals across chip



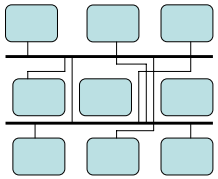
Source: Pham et al ISSCC 2005

The SoC nightmare

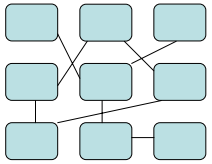


Source: Prof Jan Rabaey CS-252-2000 UC Berkeley

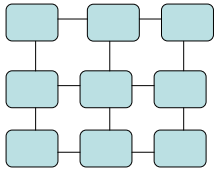
On-chip Communication



Bus-based architectures



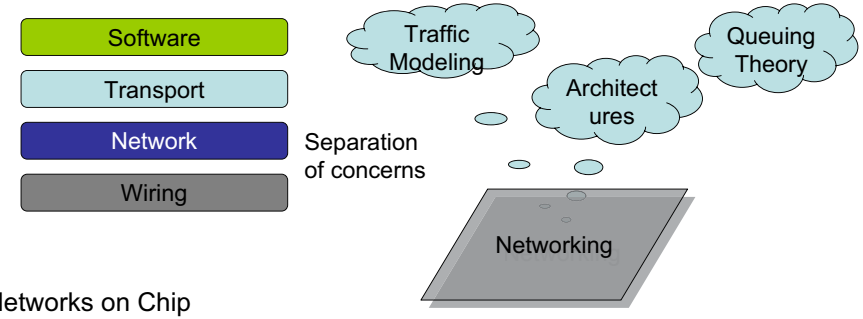
Irregular architectures



Regular Architectures

- Bus based interconnect
  - Low cost
  - Easier to Implement
  - Flexible
- Networks on Chip
  - Layered Approach
  - Buses replaced with Networked architectures
    - Better electrical properties
    - Higher bandwidth
    - Energy efficiency
    - Scalable

Network on Chip



Networks on Chip
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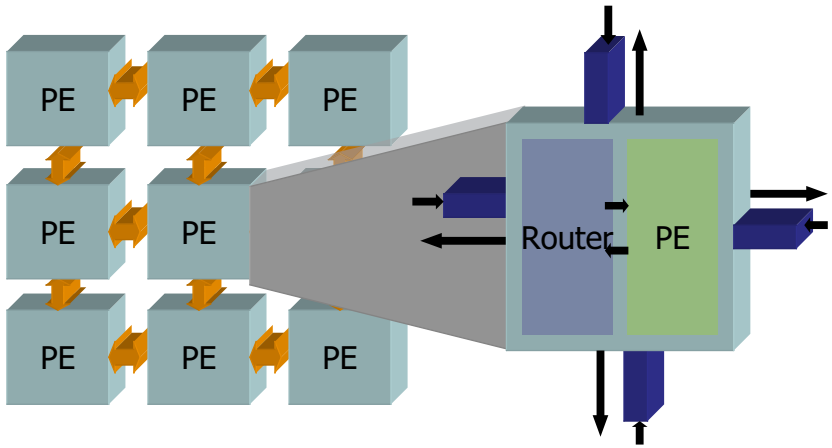
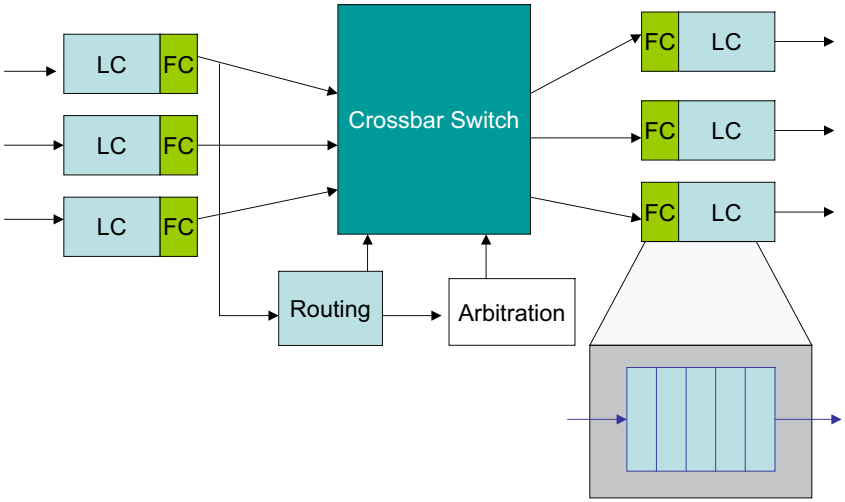
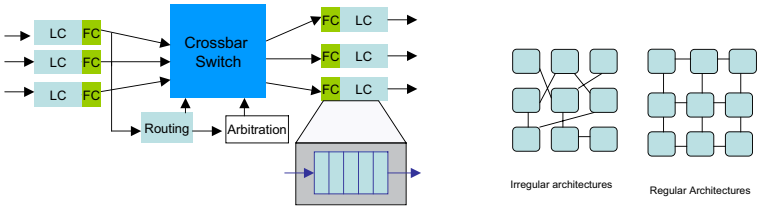
Regular Network on Chip



Typical NoC Router



NoC Issues



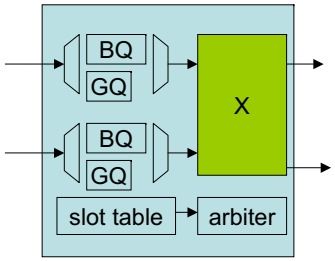
- Application Specific Optimization
  - Buffers
  - Routing
  - Topology
  - Mapping to topology
  - Implementation and Reuse

NoC Issues

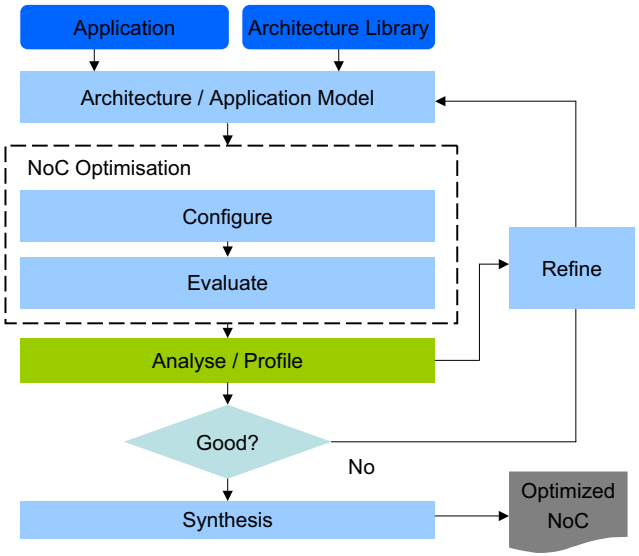
- Architecture
  - QoS Support
  - What topology will suit a particular application?
- Fault tolerance
  - Gossiping architectures

o1	o2	o3	o4
-	-	-	-
-	I1	-	-
-	I1	-	-
-	-	-	-

o1	o2	o3	o4
-	I1	-	-
-	I3	-	I1
-	-	-	-
-	-	-	-

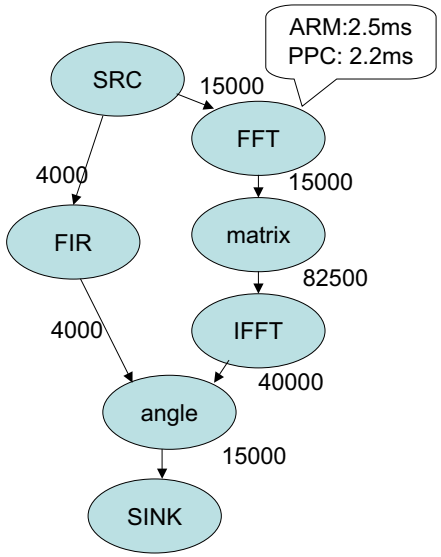


Communication Centric Design



How are application described?

- Few multiprocessor embedded benchmarks
- Task graphs
  - Extensively used in scheduling research
    - Each node has computation properties
    - Directed edge describes task dependences
    - Edge properties has communication volume

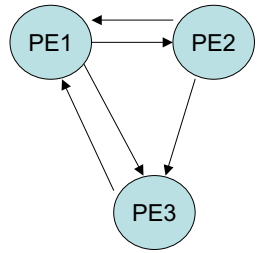


Simplifying Application Model

- With simple energy model,

  $E_{bit} = n_{hops} \times E_{Sbit} + (n_{hops} - 1) \times E_{Lbit}$

  - n_{hops} proportional to energy consumption
  - Can abstract communication design problem to



Simple Router Energy Models

- Hu et al assume:
- $E_{bit} = E_{Sbit} + E_{Bbit} + E_{Wbit} + E_{Lbit}$
- Simplifying assumptions:
  - Buffer implemented using latches and flip-flops
  - Negligible Internal wire energy

  => $E_{bit} = E_{Sbit} + E_{Bbit} + E_{Wbit} + E_{Lbit}$
- Router to Router Energy (minimal routing)
  - $E_{bit} = n_{hops} \times E_{Sbit} + (n_{hops} - 1) \times E_{Lbit}$

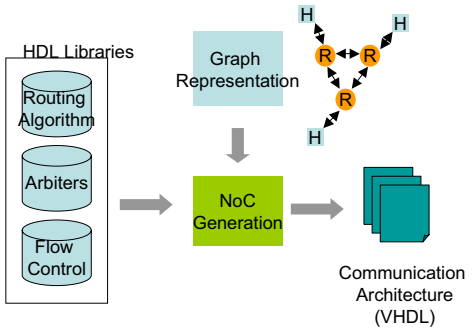
Energy-Aware Task mapping

- Reduce Energy Consumption by placing
- Addressed by Hu et al 2002:
  - Given a CTG and a heterogenous NoC
- Find:
  - A mapping function M : tasks(T) => PEs (P)
  - Assuming the tasks are already scheduled and partitioned
- Solution formulated as a quadratic assignment problem and solved using Branch and Bound with heuristics

Energy Model Limitations

- Ignore:
  - Static energy i.e. leakage power
  - Clock energy – flip flops, latches need to be clocked
- Buffering Energy is not free
  - can consume 50-80% of total communication architecture depending on size and depth of FIFOs

NoC Generation

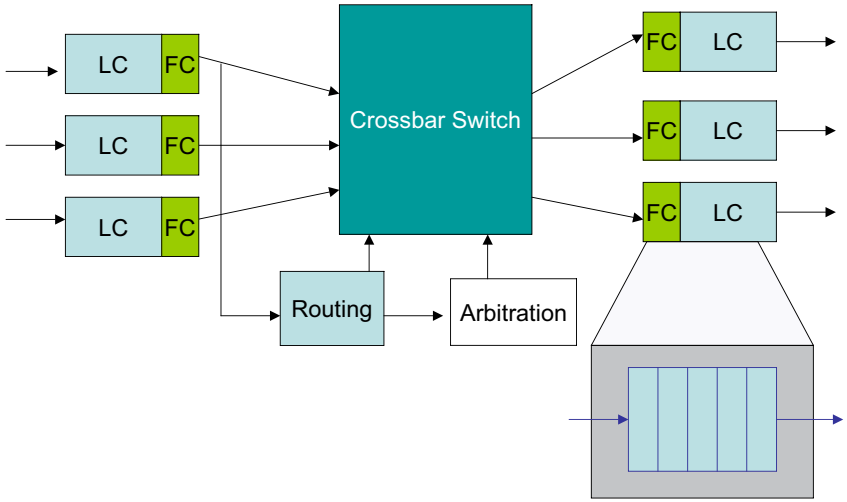


- Given a parameterized NoC architecture and library of NoC components, generate a synthesizable HDL model.

NoC Generation

- Most packet switched routers contain similar components that are connected
- Can be easily modularized to allow automatic generation

Typical NoC Router



Current Research

- Irregular Topology Generation
  - Formulated as MILP problems
  - Genetic algorithm Solution
- Buffer Allocation Problem
  - Assumed Poisson Distributed Traffic
  - Used Queuing Theory to Determine Ideal Buffering for Ports => non uniform buffering depths
- Integrated solution to optimization problems

Summary

- NoC is an exciting research area that will lead to an paradigm shift in SoC design.
- NoC research is still in infancy
  - Many open research problems
  - Need better application and traffic models, new optimization techniques
- New Power, Performance, Traffic Models being developed

Thank You