COMP4161: Advanced Topics in Software Verification

$P || Q$

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S2/2018

Content

- ➜ Intro & motivation, getting started [1]
- ➜ Foundations & Principles
  - Lambda Calculus, natural deduction [1,2]
  - Higher Order Logic [3[a]]
  - Term rewriting [4]
- ➜ Proof & Specification Techniques
  - Inductively defined sets, rule induction [5]
  - Datatypes, recursion, induction [6, 7]
  - Hoare logic, proofs about programs, invariants [8[b],9]
  - (mid-semester break)
  - C verification [10]
  - CakeML, Isar [11[c]]
  - Concurrency [12]

[a] a1 due; [b] a2 due; [c] a3 due

Program verification so far

If the following true?

$\{x = 0\}$
$y := x;$
$x := x + 1;$
$\{x = 1 \wedge y = 0\}$

Program verification so far

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YES!

Program verification with concurrency

Is it still true?

$$\{x = 0\}$$
$$y := x; \qquad || \quad x := 4$$
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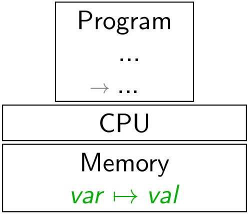
NO!

Program verification so far

So far we have assumed **sequential execution**

$\{x = 0\}$
$y := x;$
$x := x + 1;$
$\{x = 1 \land y = 0\}$

i.e. a single thread of execution accessing the memory state



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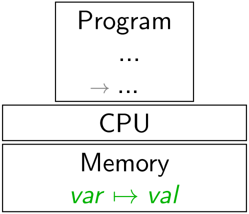

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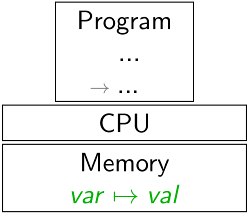
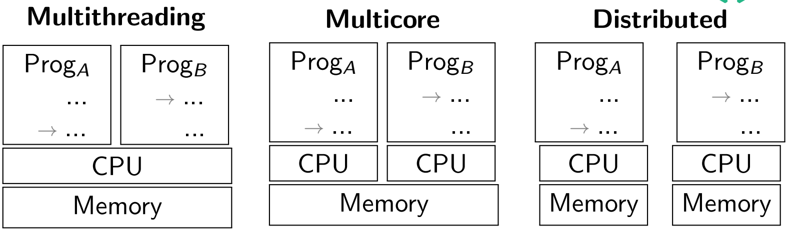


This is not always the case!

Types of concurrency



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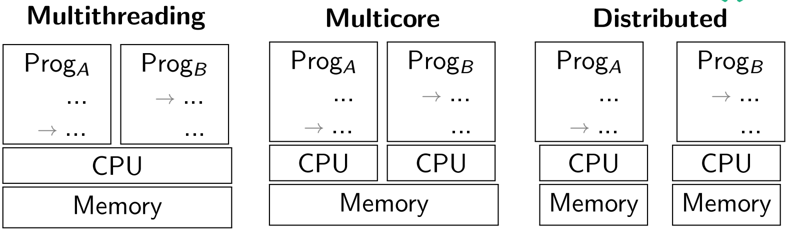
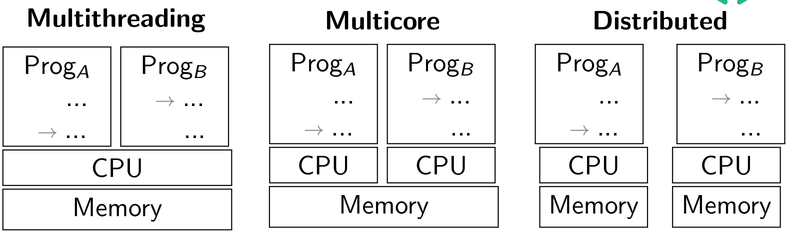


All need communication and synchronisation mechanisms

Shared memory | Shared memory | Message passing

Types of concurrency



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Multithreading	Multicore	Distributed
Shared memory Interleaved execution	Shared memory Parallel execution	Message passing

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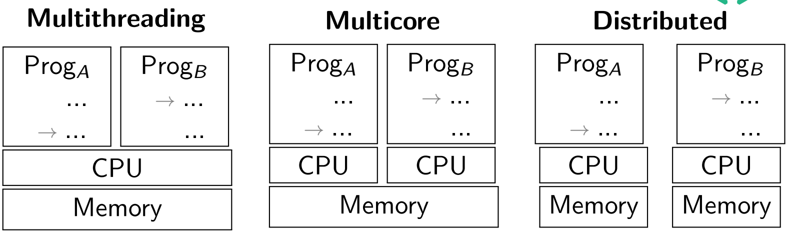

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Here: we'll look at shared-memory concurrency

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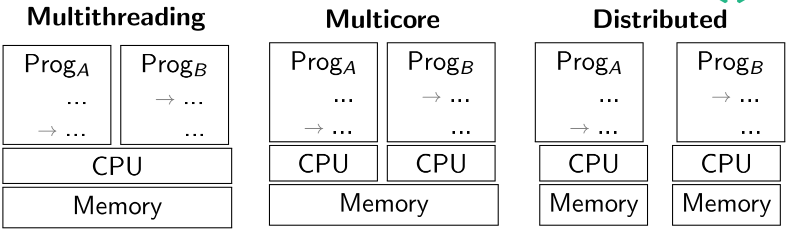

All need communication and synchronisation mechanisms

Multithreading	Multicore	Distributed
Shared memory Interleaved execution	Shared memory Parallel execution	Message passing

Here: we'll look at shared-memory concurrency

(and we'll ignore further complications such as caches, weak memory...)

Goal

We want to be able to reason about parallel composition of programs:

Prog_A		Prog_B
$\ldots$	$\|\|$	$\rightarrow \ldots$
$\rightarrow \ldots$		$\ldots$

Goal

We want to be able to reason about parallel composition of programs:

$\{precondition\}$

Prog_A		Prog_B
$\dots$	$\parallel$	$\rightarrow \dots$
$\rightarrow \dots$		$\dots$

$\{postcondition\}$

Goal

We want to be able to reason about parallel composition of programs:

$$\{\textit{precondition}\}$$

$$\boxed{\begin{array}{r}\text{Prog}_A \\ \ldots \\ \rightarrow \ldots\end{array}} \quad || \quad \boxed{\begin{array}{r}\text{Prog}_B \\ \rightarrow \ldots \\ \ldots\end{array}}$$

$$\{\textit{postcondition}\}$$

2 kinds of properties:

Safety:
"something bad does not happen"
(no bad state can be reached)

Liveness:
"something good must happen"
(specific states must be reached)

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e.g. $\{x = 0\}$

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e.g. the program terminates

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We want to be able to reason about parallel composition of programs:

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$$\{\textit{postcondition}\}$$

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With concurrency: much harder!
(set of reachable states much bigger)

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e.g. the program terminates

With concurrency: much harder!
(set of reachable states much bigger)

With concurrency: new problems!
(dead-locks, live-locks...)

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$$\{\mathit{postcondition}\}$$

Here:

- ➜ We focus on **safety** properties: postcondition holds **if reached**

Goal

We want to be able to reason about parallel composition of programs:

$\{\textit{precondition}\}$

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$\dots$	$\|\|$	$\rightarrow \dots$
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Here:

- ➜ We focus on **safety** properties: postcondition holds **if reached**
- ➜ We will define parallel composition ($||$) as non-deterministic interleaving

Goal

We want to be able to reason about parallel composition of programs:

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Here:

- ➜ We focus on **safety** properties: postcondition holds **if reached**
- ➜ We will define parallel composition ($||$) as non-deterministic interleaving
- ➜ We go back to our minimal IMP language (forget about C and monads)

```
datatype com  =   SKIP
              |   Assign vname aexp       (_ := _)
              |   Semi com com            (_; _)
              |   Cond bexp com com       (IF _ THEN _ ELSE _)
              |   While bexp com          (WHILE _ DO _ OD)
```

Program verification so far

If the following true?

$$\{x = 0\}$$
$$y := x;$$
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YES!

Program verification with concurrency

Is it still true?

$$\{x = 0\}$$
$$y := x; \qquad || \quad x := 4$$
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NO!

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Is it still true?

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NO!

What is going wrong?
What do we need to change?

- ➜ to make sure we don't prove wrong statements!
- ➜ to allow us to prove true statements about concurrent programs

Program verification so far

How would we have proved this?

$\{x = 0\}$
$y := x;$
$x := x + 1;$
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Program verification so far

How would we have proved this? Using Hoare logic rules!

$\{x = 0\}$
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Program verification so far

How would we have proved this?

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Using Hoare logic rules!

$$\frac{\vdash \ \{P\}\ c_1\ \{R\} \quad \vdash \ \{R\}\ c_2\ \{Q\}}{\vdash \ \{P\} \quad c_1; c_2 \quad \{Q\}}$$

$$\frac{}{\vdash \ \{P[x \mapsto e]\} \quad x := e \quad \{P\}}$$

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$\{x = 0\} \implies \{x + 1 = 1 \wedge x = 0\}$
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Why does this make it true? What does it mean that it's true?

It means:

If the program "$y := x;\ x := x + 1$" is executed from a state satisfying $\{x = 0\}$ then, if it terminates, the resulting state satisfied $\{x = 1 \wedge y = 0\}$

Program verification so far

How would we have proved this?

$\{x = 0\} \quad \Longrightarrow \{x + 1 = 1 \wedge x = 0\}$
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$$\langle y := x;\ x := x + 1, \sigma\rangle \rightarrow \sigma' \quad \wedge \quad x\ \sigma = 0 \quad \longrightarrow \quad x\ \sigma' = 1\ \wedge\ y\ \sigma' = 0$$

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Where:

$$\frac{\langle c_1, \sigma\rangle \rightarrow \sigma' \quad \langle c_2, \sigma'\rangle \rightarrow \sigma''}{\langle c_1; c_2, \sigma\rangle \rightarrow \sigma''} \qquad \frac{e\ \sigma = v}{\langle \mathrm{x} := \mathrm{e}, \sigma\rangle \rightarrow \sigma[x \mapsto v]}$$

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Soundness: $\vdash \{P\}\ c\ \{Q\} \Longrightarrow \forall \sigma\ \sigma'.\ \langle c, \sigma\rangle \to \sigma' \wedge P\ \sigma \longrightarrow Q\ \sigma'$

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What changes when we have another program running in parallel?

Program verification with concurrency

$$\{x = 0\}$$
$$y := x;\ \cancel{\{x + 1 = 1 \wedge y = 0\}} \quad || \quad x := 4$$
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Program verification with concurrency

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➜ Execution is interleaved; Intermediate assertions can be interferred with

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➜ Execution is interleaved; Intermediate assertions can be interferred with

➜ Need a new reasoning framework!

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➜ New syntax, new semantics,
new proof rules (proved sound w.r.t semantics), new VCG

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➜ (1969: Hoare Logic (Tony Hoare))

➜ 1976: Owicki-Gries (Susan Owicki and David Gries)

➜ 1981: Rely-Guarantee (Cliff Jones)

➜ ...

Program verification with concurrency

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- ➜ ...

OG+RG formalised in Isabelle/HOL by Leonor Prensa Nieto, 2002

Owicki-Gries framework

Intuition:

- Syntax: our IMP language + Parallel operator + Await operator
- Semantics:
  - $P \mid\mid Q$: pick one program and execute its current instruction
  - $AWAIT\ b\ DO\ c\ OD$: if guard is true execute c atomically

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$$
\begin{array}{l|l}
\{is\_even\ x\} & \\
x := x + 1; & x := x + 2 \\
x := x + 1; & \\
\{is\_even\ x\} &
\end{array}
$$

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$$\begin{array}{l} \{\mathit{is\_even}\ x\} \\ x := x + 1;\ \{\mathit{is\_even}\ x + 1\} \\ x := x + 1; \\ \{\mathit{is\_even}\ x\} \end{array} \;\Bigg\|\; x := x + 2$$

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➜ **Needs a fully annotated program!**

➜ **Needs a "small-step semantics"** $\langle c, \sigma \rangle \rightarrow \langle c', \sigma' \rangle$
(before big-step: $\langle c, \sigma \rangle \rightarrow \sigma'$)

Owicki-Gries framework

Formally:

- Syntax: our IMP language + Parallel operator + Await operator
- Semantics:

$$\frac{\langle c_1, \sigma \rangle \rightarrow \langle c_1', \sigma' \rangle}{\langle c_1 || c_2, \sigma \rangle \rightarrow \langle c_1' || c_2, \sigma' \rangle} \quad \frac{\langle c_2, \sigma \rangle \rightarrow \langle c_2', \sigma' \rangle}{\langle c_1 || c_2, \sigma \rangle \rightarrow \langle c_1 || c_2', \sigma' \rangle}$$

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- Hoare rules:

$$\frac{\{P_1\}\ c_1\ \{Q_1\} \quad \{P_2\}\ c_2\ \{Q_2\} \quad \mathit{interfree}\ c_1\ c_2 \quad \mathit{interfree}\ c_2\ c_1}{\{P_1 \wedge P_2\}\ c_1 || c_2\ \{Q_1 \wedge Q_2\}}$$

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Where

$\mathit{interfree}\ c_1\ c_2 \equiv$

$\forall p \in (\mathit{assertions}\ c_1).\ \forall (a, c) \in (\mathit{atomics}\ c_2).\ \{p \wedge a\} c \{p\}$

Owicki-Gries framework

➜ **Quadratic explosion of proof obligations! (verification conditions)**
➜ **Not compositional**
➜ **Not complete:** sometimes need auxilliary/ghost variables

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➜ **Quadratic explosion of proof obligations! (verification conditions)**
➜ **Not compositional**
➜ **Not complete:** sometimes need auxilliary/ghost variables

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$$x := x + 1; \parallel x := x + 1$$
$$\{x = 2\}$$

$$\{x = 0 \wedge a_1 = 0 \wedge a_2 = 0\}$$

$$< x := x + 1; a_1 := 1 > \parallel < x := x + 1; a_2 := 1 >$$

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Demo

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Intuition:

- Syntax, semantics: as before (but no need for assertions)
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$$\underset{P}{\sigma_0} \overset{c}{\rightarrow} \sigma_1 \overset{c}{\rightarrow} \sigma_2 \underset{R}{\overset{c'}{\rightarrow}} \sigma_3 \overset{c}{\rightarrow} \sigma_4 \underset{R}{\overset{c'}{\rightarrow}} \sigma_5 \underset{R}{\overset{c'}{\rightarrow}} \sigma_6 \overset{c}{\rightarrow} \underset{Q}{\sigma_7}$$

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Where $\mathit{stable}\ P\ R\ =\ \forall\ \sigma\ \sigma'.\ (P\sigma \wedge R(\sigma, \sigma')) \rightarrow P\sigma'$
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$$\frac{c_1\{P_1, R_1, G_1, Q_1\} \quad c_2\{P_2, R_2, G_2, Q_2\} \quad G_1 \subseteq R_2 \quad G_2 \subseteq R_1}{c_1 || c_2\{P_1 \cap P_2, R_1 \cap R_2, G_1 \cup G_2, Q_1 \cap Q_2\}}$$

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Intuition: the guarantee of one program is the rely of the other program

Demo

We have seen today ...

- Need for new reasoning framework for parallel/concurrent programs
- Owicki-Gries
- Rely-Guarantee