I/O Management

Intro

Chapter 5 - 5.3

Learning Outcomes

• A high-level understanding of the properties of a variety of I/O devices.
• An understanding of methods of interacting with I/O devices.

I/O Devices

• There exists a large variety of I/O devices:
  – Many of them with different properties
  – They seem to require different interfaces to manipulate and manage them
    • We don’t want a new interface for every device
    • Diverse, but similar interfaces leads to code duplication
  • Challenge:
    – Uniform and efficient approach to I/O

Device Drivers

• Logical position of device drivers is shown here
• Drivers (originally) compiled into the kernel
  – Including OS/161
  – Device installers were technicians
  – Number and types of devices rarely changed
• Nowadays they are dynamically loaded when needed
  – Linux modules
  – Typical users (device installers) can’t build kernels
  – Number and types vary greatly
    • Even while OS is running (e.g. hot-plug USB devices)

• Drivers classified into similar categories
  – Block devices and character (stream of data) devices
• OS defines a standard (internal) interface to the different classes of devices
  – Example: USB Human Input Device (HID) class specifications
  • Human input devices follow a set of rules making it easier to design a standard interface.
USB Device Classes

<table>
<thead>
<tr>
<th>Base</th>
<th>Usage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>Device</td>
<td>Use class information in the Interface Descriptors</td>
</tr>
<tr>
<td>01h</td>
<td>Interface Audio</td>
<td></td>
</tr>
<tr>
<td>02h</td>
<td>Both Communications and CDC Control</td>
<td></td>
</tr>
<tr>
<td>03h</td>
<td>Interface HID (Human Interface Device)</td>
<td></td>
</tr>
<tr>
<td>05h</td>
<td>Interface Physical</td>
<td></td>
</tr>
<tr>
<td>06h</td>
<td>Interface Image</td>
<td></td>
</tr>
<tr>
<td>07h</td>
<td>Interface Printer</td>
<td></td>
</tr>
<tr>
<td>08h</td>
<td>Interface Mass Storage</td>
<td></td>
</tr>
<tr>
<td>09h</td>
<td>Device Hub</td>
<td></td>
</tr>
<tr>
<td>0Ah</td>
<td>Interface CDC-Data</td>
<td></td>
</tr>
<tr>
<td>0Bh</td>
<td>Interface Smart Card</td>
<td></td>
</tr>
<tr>
<td>0Dh</td>
<td>Interface Content Security</td>
<td></td>
</tr>
<tr>
<td>0Eh</td>
<td>Interface Video</td>
<td></td>
</tr>
<tr>
<td>0Fh</td>
<td>Interface Personal Healthcare</td>
<td></td>
</tr>
<tr>
<td>10h</td>
<td>Interface Audio/Video Devices</td>
<td></td>
</tr>
<tr>
<td>DCh</td>
<td>Both Diagnostic Device</td>
<td></td>
</tr>
<tr>
<td>E0h</td>
<td>Interface Wireless Controller</td>
<td></td>
</tr>
<tr>
<td>EFh</td>
<td>Both Miscellaneous</td>
<td></td>
</tr>
<tr>
<td>FEh</td>
<td>Interface Application Specific</td>
<td></td>
</tr>
<tr>
<td>FFh</td>
<td>Both Vendor Specific</td>
<td></td>
</tr>
</tbody>
</table>

I/O Device Handling

- **Data rate**
  - May be differences of several orders of magnitude between the data transfer rates
  - Example: Assume 1000 cycles/byte I/O
    - Keyboard needs 10 KHz processor to keep up
    - Gigabit Ethernet needs 100 GHz processor…..

Sample Data Rates

<table>
<thead>
<tr>
<th>Device</th>
<th>Data rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Keyboard</td>
<td>10 bytes/second</td>
</tr>
<tr>
<td>Mouse</td>
<td>100 bytes/second</td>
</tr>
<tr>
<td>SD card</td>
<td>7 MB/s</td>
</tr>
<tr>
<td>Telephone channel</td>
<td>8 MB/s</td>
</tr>
<tr>
<td>Dustbin fans</td>
<td>18 MB/s</td>
</tr>
<tr>
<td>Laser printer</td>
<td>100 MB/s</td>
</tr>
<tr>
<td>DVI monitor</td>
<td>40 MB/s</td>
</tr>
<tr>
<td>Gigabit Ethernet</td>
<td>1 Gb/s</td>
</tr>
<tr>
<td>USB Universal Serial Bus</td>
<td>1.5 MB/s</td>
</tr>
<tr>
<td>Digital cord/line</td>
<td>8 MB/s</td>
</tr>
<tr>
<td>Ethernet</td>
<td>5 MB/s</td>
</tr>
<tr>
<td>eSATA</td>
<td>16.7 MB/s</td>
</tr>
<tr>
<td>IDE (ATA/2) disk</td>
<td>16.7 MB/s</td>
</tr>
<tr>
<td>Firewire (1394)</td>
<td>50 MB/s</td>
</tr>
<tr>
<td>VGA Monitor</td>
<td>80 MB/s</td>
</tr>
<tr>
<td>SATA H-DC-37 connector</td>
<td>70 MB/s</td>
</tr>
<tr>
<td>USB 2.0</td>
<td>60 MB/s</td>
</tr>
<tr>
<td>PCIe x16</td>
<td>160 MB/s</td>
</tr>
<tr>
<td>Digital optical</td>
<td>50 MB/s</td>
</tr>
<tr>
<td>Optical drive</td>
<td>40 MB/s</td>
</tr>
<tr>
<td>iPod</td>
<td>300 MB/s</td>
</tr>
<tr>
<td>SD card</td>
<td>200 MB/s</td>
</tr>
</tbody>
</table>

Device Drivers

- **Device drivers’ job**
  - Translate requests through the device-independent standard interface (open, close, read, write) into appropriate sequence of commands (register manipulations) for the particular hardware
  - Initialise the hardware at boot time, and shut it down cleanly at shutdown

Device Driver

- **After issuing the command to the device, the device either**
  - Completes immediately and the driver simply returns to the caller
  - Or, device must process the request and the driver usually blocks waiting for an I/O complete interrupt.
- **Drivers are thread-safe** as they can be called by another process while a process is already blocked in the driver.
  - Thread-safe: Synchronised…

Device-Independent I/O Software

- There is commonality between drivers of similar classes
- Divide I/O software into device-dependent and device-independent I/O software
- Device independent software includes
  - Buffer or Buffer-cache management
  - TCP/IP stack
  - Managing access to dedicated devices
  - Error reporting
Driver ⇔ Kernel Interface

- Major Issue is uniform interfaces to devices and kernel
  - Uniform device interface for kernel code
    - Allows different devices to be used the same way
    - No need to rewrite file-system to switch between SCSI, IDE or RAM disk
    - Allows internal changes to device driver with fear of breaking kernel code
  - Uniform kernel interface for device code
    - Drivers use a defined interface to kernel services (e.g. kmalloc, install IRQ handler, etc.)
    - Allows kernel to evolve without breaking existing drivers
  - Together both uniform interfaces avoid a lot of programming implementing new interfaces
    - Retains compatibility as drivers and kernels change over time.

Accessing I/O Controllers

a) Separate I/O and memory space
   - I/O controller registers appear as I/O ports
   - Accessed with special I/O instructions
b) Memory-mapped I/O
   - Controller registers appear as memory
   - Use normal load/store instructions to access
c) Hybrid
   - x86 has both ports and memory mapped I/O

Bus Architectures

(a) A single-bus architecture
(b) A dual-bus memory architecture

Interrupts

- Devices connected to an Interrupt Controller via lines on an I/O bus (e.g. PCI)
- Interrupt Controller signals interrupt to CPU and is eventually acknowledged.
- Exact details are architecture specific.

Intel IXP420

I/O Interaction
Programmed I/O
• Also called polling, or busy waiting
• I/O module (controller) performs the action, not the processor
• Sets appropriate bits in the I/O status register
• No interrupts occur
• Processor checks status until operation is complete – Wastes CPU cycles

Interrupt-Driven I/O
• Processor is interrupted when I/O module (controller) ready to exchange data
• Processor is free to do other work
• No needless waiting
• Consumes a lot of processor time because every word read or written passes through the processor

Direct Memory Access
• Transfers data directly between Memory and Device
• CPU not needed for copying

Direct Memory Access
• Transfers a block of data directly to or from memory
• An interrupt is sent when the task is complete
• The processor is only involved at the beginning and end of the transfer

DMA Considerations
✓ Reduces number of interrupts
  – Less (expensive) context switches or kernel entry-exits
× Requires contiguous regions (buffers)
  – Copying
  – Some hardware supports “Scatter-gather”
• Synchronous/Asynchronous
• Shared bus must be arbitrated (hardware)
  – CPU cache reduces (but not eliminates) CPU need for bus

The Process to Perform DMA Transfer
1. DMA controller initiates DMA transfer
2. DMA controller requests DMA transfer
3. DMA controller initiates DMA transfer
4. DMA controller sends DMA buffer to DMA controller

CPU
Memory
Device

CPU
Memory
Device

CPU
Memory
Device

CPU
Memory
Device
Learning Outcomes

- An understanding of the structure of I/O related software, including interrupt handlers.
- An appreciation of the issues surrounding long running interrupt handlers, blocking, and deferred interrupt handling.
- An understanding of I/O buffering and buffering’s relationship to a producer-consumer problem.

Operating System Design Issues

- **Efficiency**
  - Most I/O devices slow compared to main memory (and the CPU)
    - Use of multiprogramming allows for some processes to be waiting on I/O while another process executes
    - Often I/O still cannot keep up with processor speed
    - Swapping may used to bring in additional Ready processes
      - More I/O operations
  - **Optimise I/O efficiency – especially Disk & Network I/O**

- **The quest for generality/uniformity:**
  - Ideally, handle all I/O devices in the same way
    - Both in the OS and in user applications
  - **Problem:**
    - Diversity of I/O devices
    - Especially, different access methods (random access versus stream based) as well as vastly different data rates.
    - Generality often compromises efficiency!
  - Hide most of the details of device I/O in lower-level routines so that processes and upper levels see devices in general terms such as read, write, open, close.

I/O Software Layers

```
User-level I/O software
Device-independent operating system software
Device drivers
Interrupt handlers
Hardware
```

Interrupt Handlers

- **Interrupt handlers**
  - Can execute at (almost) any time
    - Raise (complex) concurrency issues in the kernel
    - Can propagate to userspace (signals, upcalls), causing similar issues
    - Generally structured so I/O operations block until interrupts notify them of completion
      - kern/dev/lamebus/lhd.c
Interrupt Handler Example

```c
static int
lhd_io(struct device *d, struct uio *uio)
{
    ...
    /* Loop over all the sectors
     * we were asked to do. */
    for (i=0; i<len; i++)
    {
        ...
        /* Wait until nobody
         * else is using the device. */
        P(lh->lh_clear);
        ...
        /* Tell it what sector we want... */
        lhd_wreg(lh, LHD_REG_SECT, sector+i);
        /* and start the operation. */
        ...
        /* Now wait until the interrupt
         * handler tells us we’re done. */
        P(lh->lh_done);
        /* Get the result value
         * saved by the interrupt handler. */
        result = lh->lh_result;
    }
}
```

### Interrupt Handler Steps

- **Save Registers** not already saved by hardware interrupt mechanism
  - (Optionally) set up context for interrupt service procedure
    - Typically, handler runs in the context of the currently running process
    - No expensive context switch
- **Set up stack** for interrupt service procedure
  - Handler usually runs on the kernel stack of current process
  - Or “nests” if already in kernel mode running on kernel stack
- **Ack/Mask interrupt controller**, re-enable other interrupts
  - Implies potential for interrupt nesting.

### Interrupt Handler Steps

- **Run interrupt service procedure**
  - Acknowledges interrupt at device level
  - Figures out what caused the interrupt
  - Re-enabled, it signals blocked device driver
- **In some cases, will have woken up a higher priority blocked thread**
  - Choose newly woken thread to schedule next
  - Set up MMU context for process to run next
  - What if we are nested?
- **Load new/original process’ registers**
- **Re-enable interrupt**; Start running the new process

### Sleeping in Interrupts

- An interrupt generally has no context (runs on current kernel stack)
  - Unfair to sleep on interrupted process (deadlock possible)
  - Where to get context for long running operation?
  - What goes into the ready queue?
- **What to do?**
  - Top and Bottom Half
  - Linux implements with tasklets and workqueues
  - Generically, in-kernel thread(s) handle long running kernel operations.

### Top/Half Bottom Half

- **Top Half**
  - Interrupt handler
  - remains short
- **Bottom half**
  - Is preemptable by top half (interrupts)
  - Performs deferred work (e.g. IP stack processing)
  - Is checked prior to every kernel exit
  - Signals blocked processes/threads to continue
  - Enables low interrupt latency
  - Bottom half can’t block

### Stack Usage

<table>
<thead>
<tr>
<th>Stack Usage</th>
<th>Kernel Stack</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Higher-level software</td>
<td>![H]</td>
</tr>
<tr>
<td>2. Interrupt processing (interrupts disabled)</td>
<td>![H]</td>
</tr>
<tr>
<td>3. Deferred processing (interrupt re-enabled)</td>
<td>![H]</td>
</tr>
<tr>
<td>4. Interrupt while in bottom half</td>
<td>![H]</td>
</tr>
</tbody>
</table>
Deferring Work on In-kernel Threads

- Interrupt
  - Handler defers work onto in-kernel thread
- In-kernel thread handles deferred work (DW)
  - Scheduled normally
  - Can block
- Both low interrupt latency and blocking operations

Buffering

Device-Independent I/O Software

(a) Unbuffered input
(b) Buffering in user space
(c) Single buffering in the kernel followed by copying to user space
(d) Double buffering in the kernel

No Buffering

- Process must read/write a device a byte/word at a time
  - Each individual system call adds significant overhead
  - Process must wait until each I/O is complete
    - Blocking/interrupt/waking adds to overhead.
    - Many short runs of a process is inefficient (poor CPU cache temporal locality)

User-level Buffering

- Process specifies a memory buffer that incoming data is placed in until it fills
  - Filling can be done by interrupt service routine
  - Only a single system call, and block/wakeup per data buffer
    - Much more efficient

User-level Buffering

- Issues
  - What happens if buffer is paged out to disk
    - Could lose data while unavailable buffer is paged in
  - Could lock buffer in memory (needed for DMA), however many processes doing I/O reduce RAM available for paging.
    - Can cause deadlock as RAM is limited resource
  - Consider write case
    - When is buffer available for re-use?
      - Either process must block until potential slow device drains buffer
      - or deal with asynchronous signals indicating buffer drained
Single Buffer

• Operating system assigns a buffer in kernel’s memory for an I/O request
• In a stream-oriented scenario
  – Used a line at a time
  – User input from a terminal is one line at a time with carriage return signaling the end of the line
  – Output to the terminal is one line at a time

Single Buffer Speed Up

• Assume
  – $T$ is transfer time for a block from device
  – $C$ is computation time to process incoming block
  – $M$ is time to copy kernel buffer to user buffer
• Computation and transfer can be done in parallel
• Speed up with buffering

$$\frac{T + C}{\max(T, C) + M}$$

Double Buffer

• Use two system buffers instead of one
• A process can transfer data to or from one buffer while the operating system empties or fills the other buffer
Double Buffer Speed Up

- Computation and Memory copy can be done in parallel with transfer
- Speed up with double buffering

\[
\frac{T + C}{\max(T, C + M)}
\]

- Usually \( M \) is much less than \( T \) giving a favourable result

Double Buffer

- May be insufficient for really bursty traffic
  - Lots of application writes between long periods of computation
  - Long periods of application computation while receiving data
  - Might want to read-ahead more than a single block for disk

Circular Buffer

- More than two buffers are used
- Each individual buffer is one unit in a circular buffer
- Used when I/O operation must keep up with process

Is Buffering Always Good?

\[
\frac{T + C}{\max(T, C) + M}
\]

- Can \( M \) be similar or greater than \( C \) or \( T \)?

Important Note

- Notice that buffering, double buffering, and circular buffering are all

Bounded-Buffer

Producer-Consumer Problems

Buffering in Fast Networks

- Networking may involve many copies
- Copying reduces performance
  - Especially if copy costs are similar to or greater than computation or transfer costs
- Super-fast networks put significant effort into achieving zero-copy
- Buffering also increases latency
I/O Software Summary

Layers of the I/O system and the main functions of each layer